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MS-7760 Ver: 2.0

CPU:

INTEL - Sandy Bridge-E LGA2011

System Chipset:

INTEL - Patsburg PCH

OnBoard Chipset:

Clock Gen:932SQ420D + 9FG1200AG-5LF

LAN:Intel PHY82579

USB3.0: UPD720200F1 X2

Flash ROM: 8 MB SPI / 8 MB SPI (PCH)

SIO:FIN71889AD(LAA)

PWM:

CPU:uP1618 (8-Dr.MOS)

CPU_SA:uP1618 (1-Dr.MOS)

CPU_VTT:UP6212 (2-Dr.MOS)

VCC_DDR:UP6212(2-Dr.MOS)

PCH:uP1508 (1-Dr.MOS)

ACPI:

UPI

Other:

SATA3.0 *2+SATA2.0 *4

USB2.0 *14 (Rear*6 Front*8)

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X8) Slot * 1

PCI Express (X1) Slot * 3

Main Memory:

DDRIII (1066/1333MHz) * 8

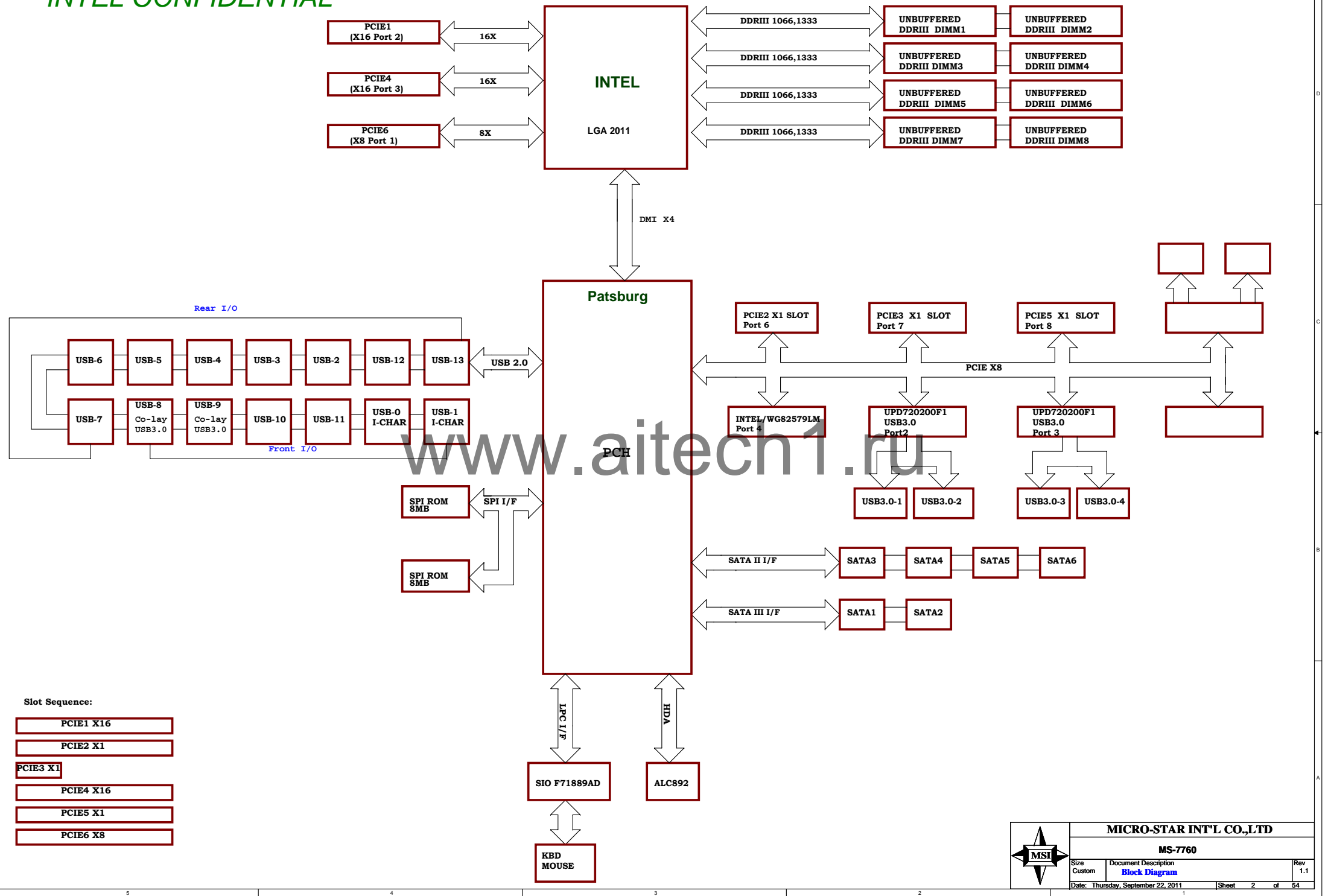
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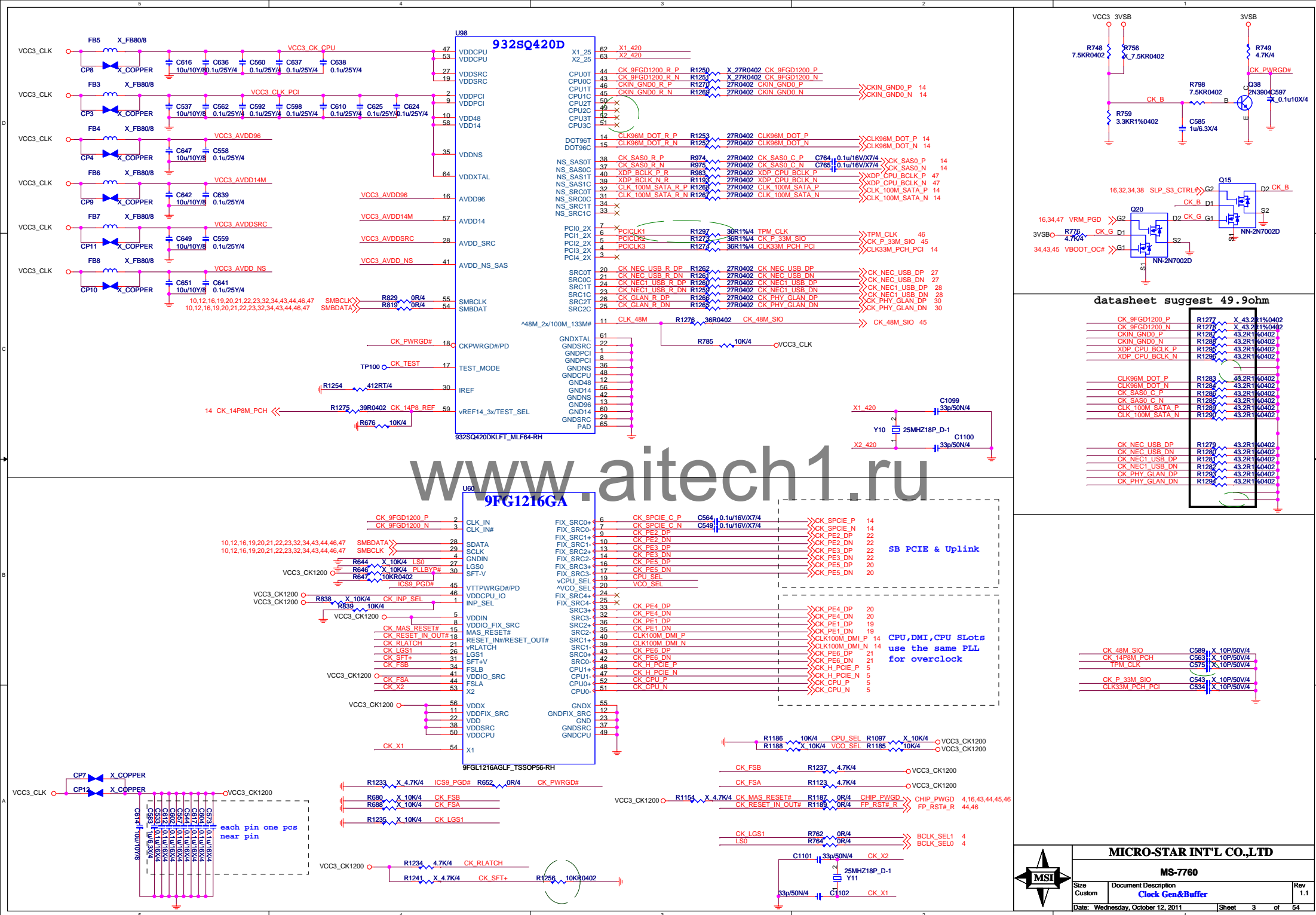


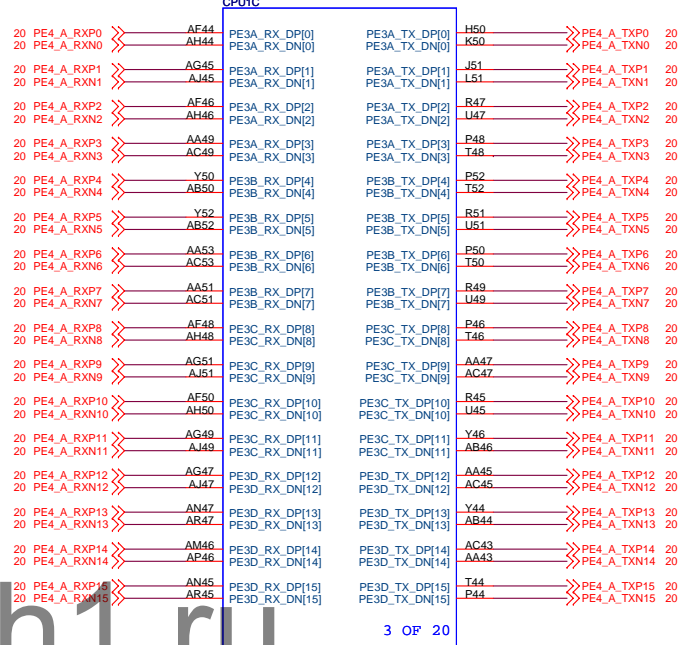
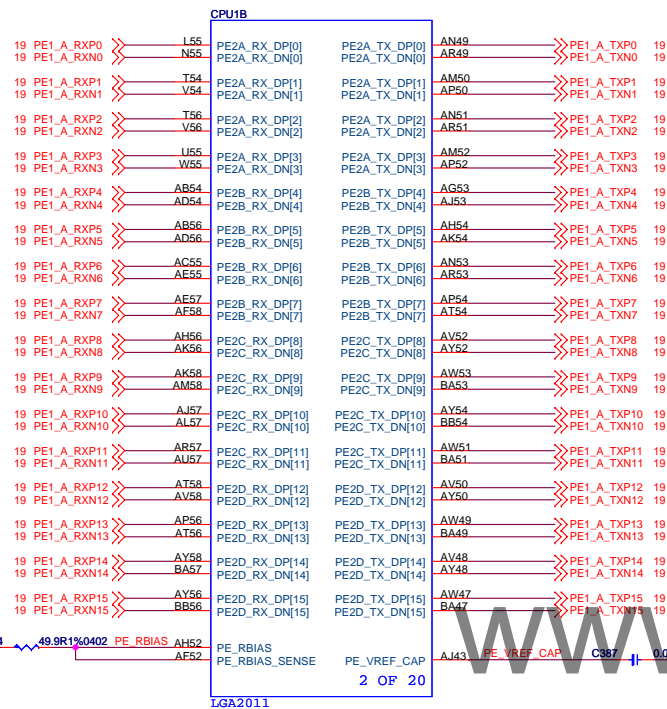
MICRO-STAR INT'L CO.,LTD

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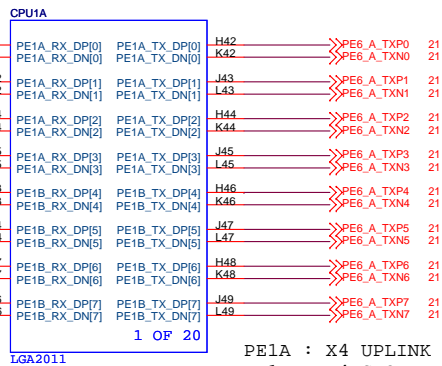
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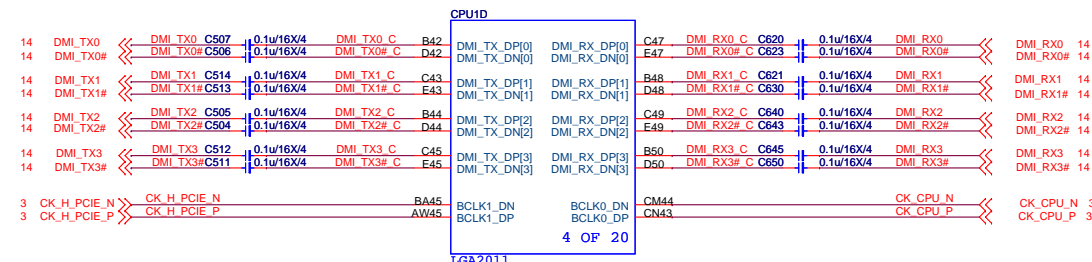




3 OF 20

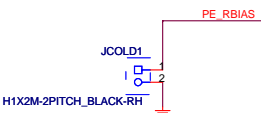



1 OF 20



4 OF 20

Reserve for Cold Bug



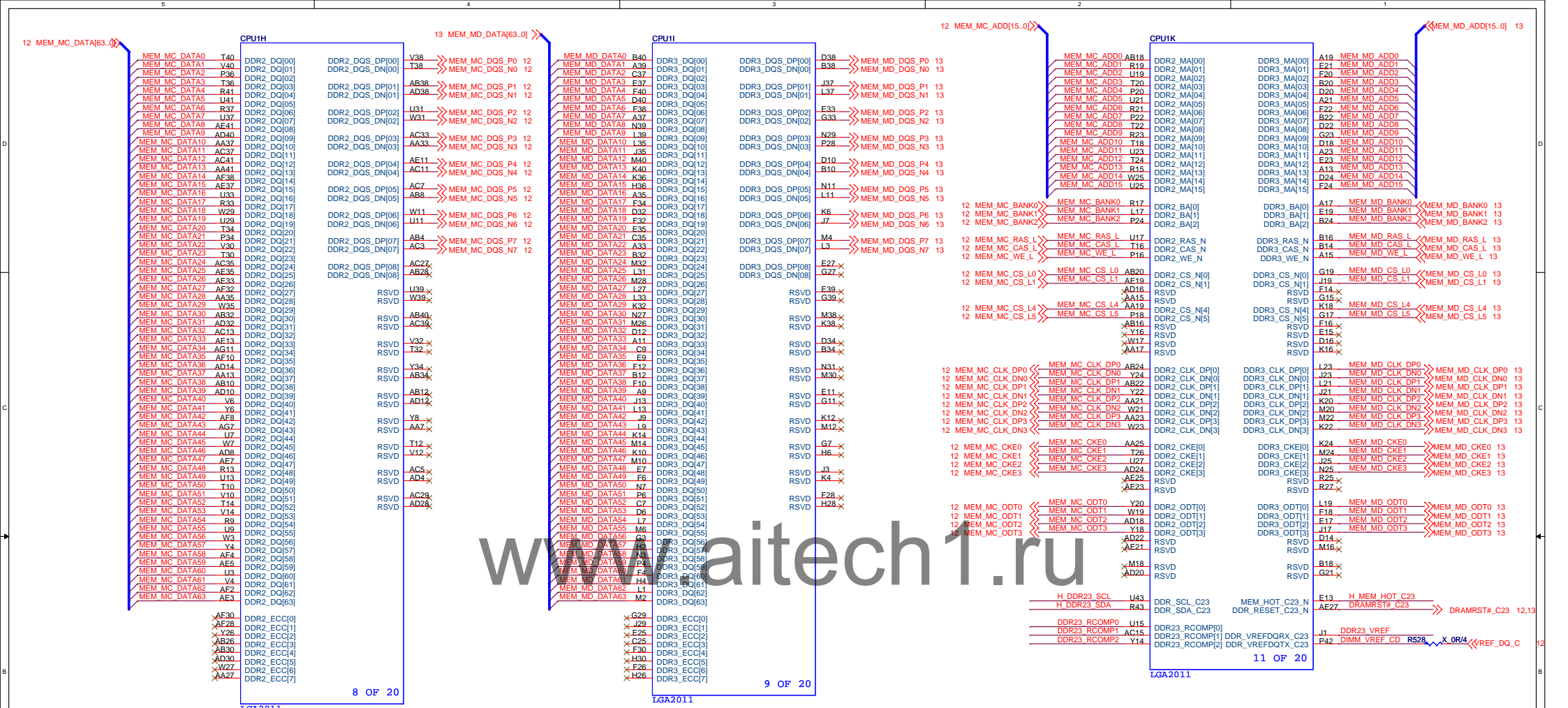


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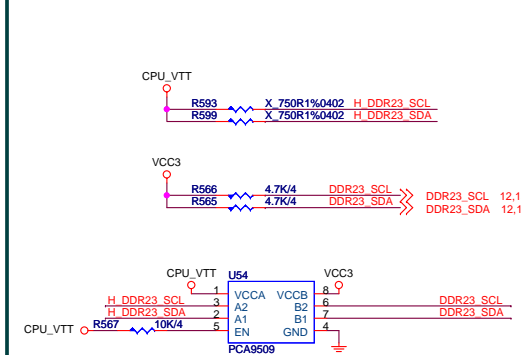
MS-7760

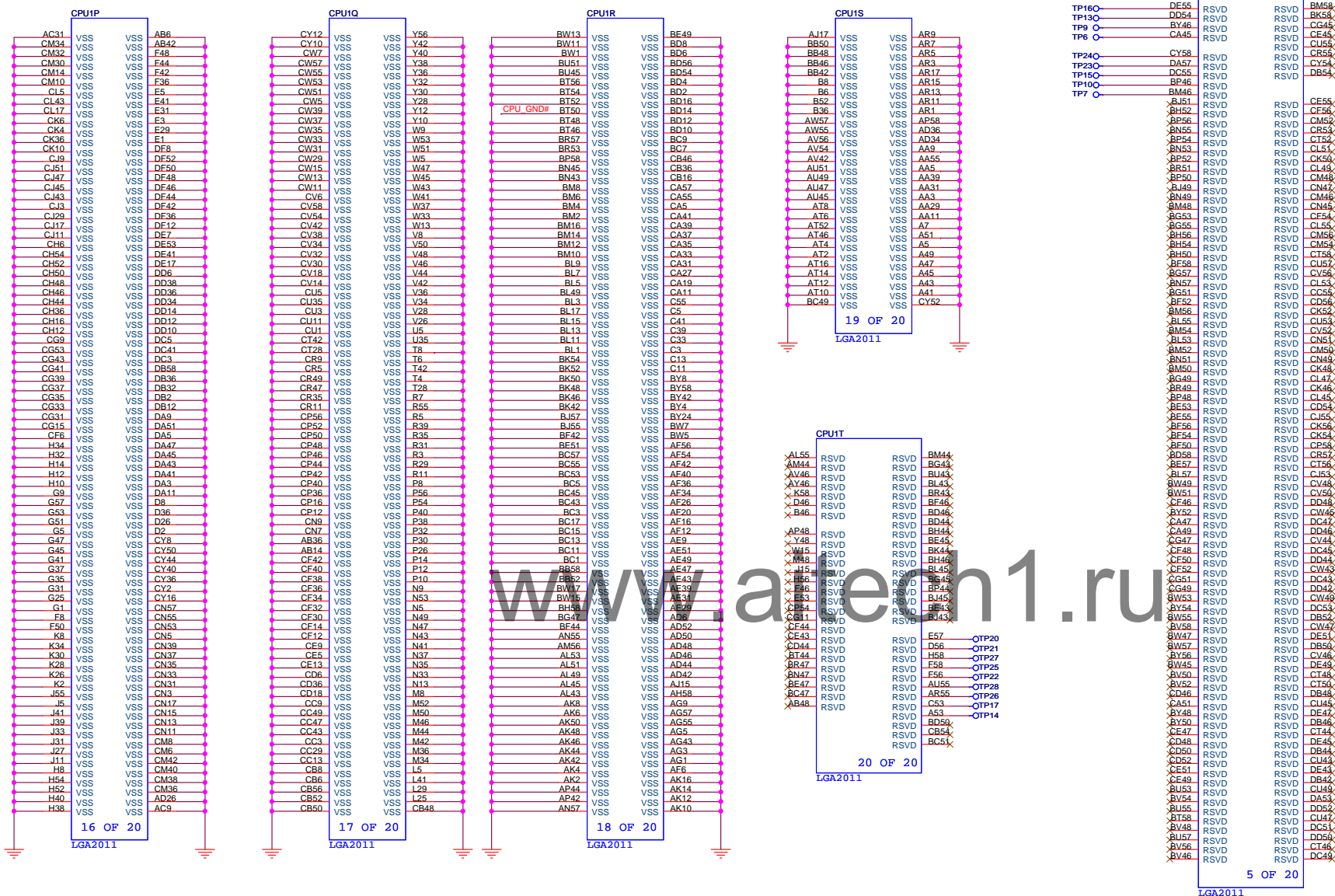
Size Custom Document Description **CPU-PEG/DMI** Rev 1.1

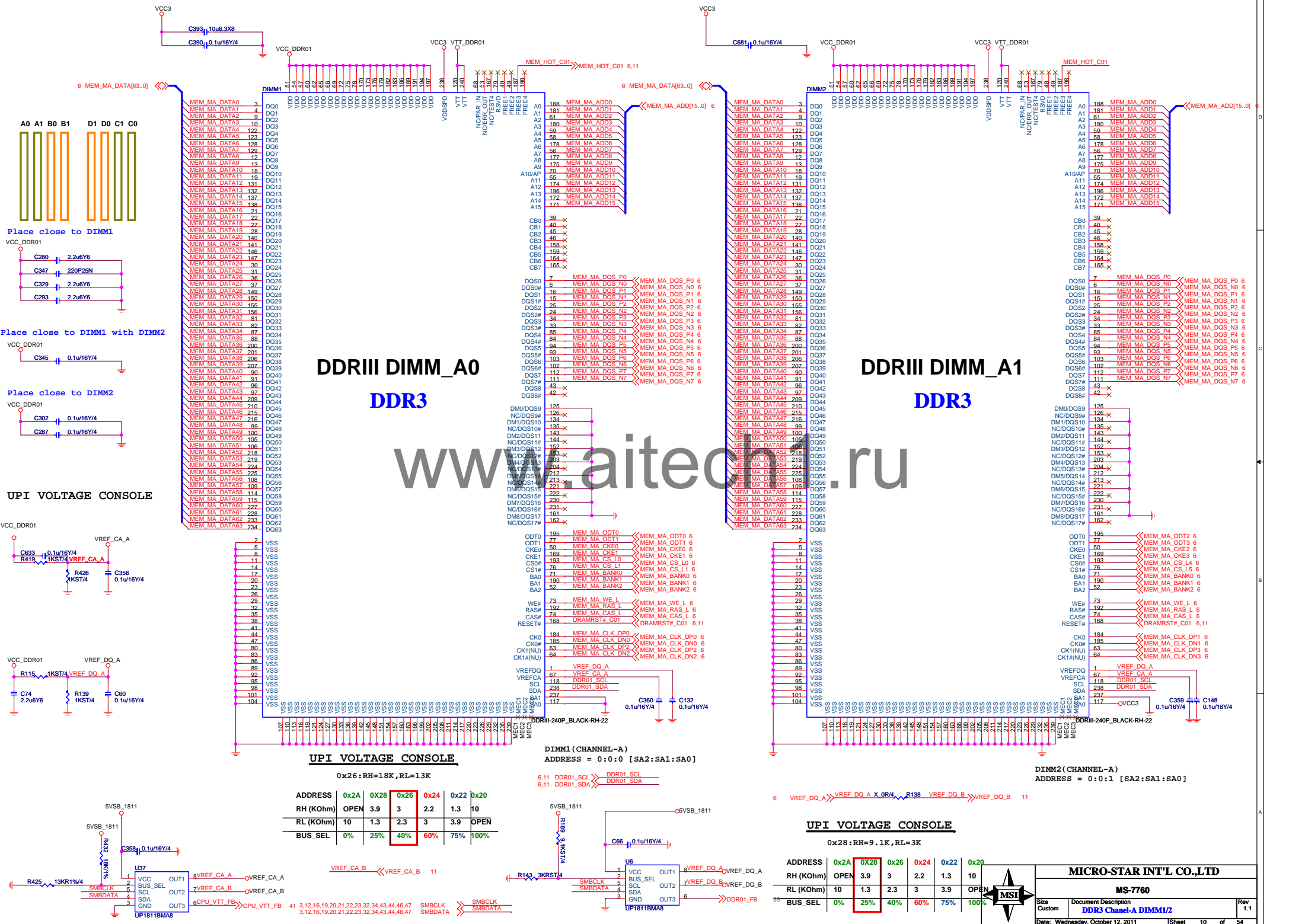
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Level Shift







DDR3 DIMM_A0

DDR3 DIMM_A1

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UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

UPI VOLTAGE CONSOLE

0x28: RH=9.1K, RL=3K

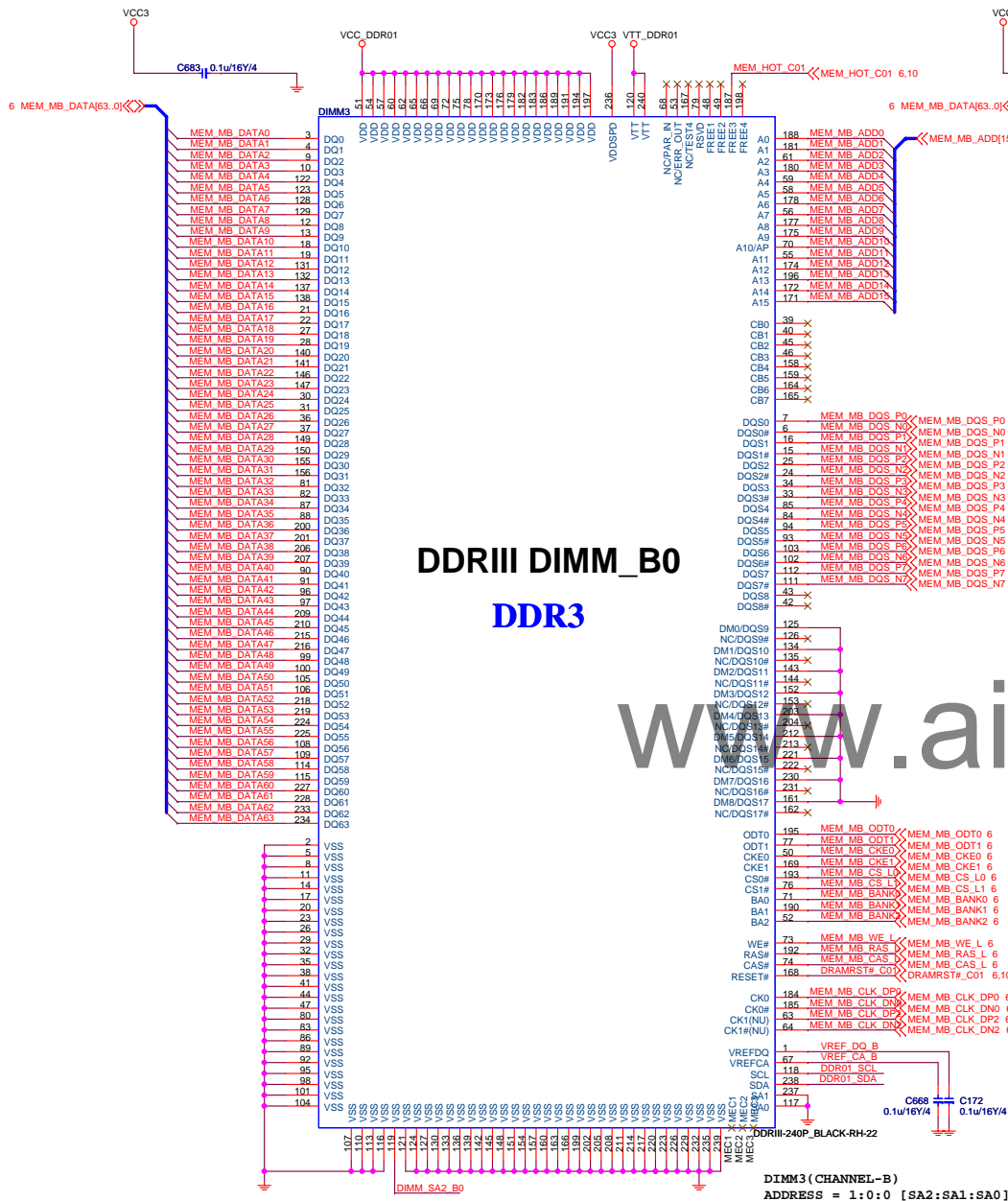
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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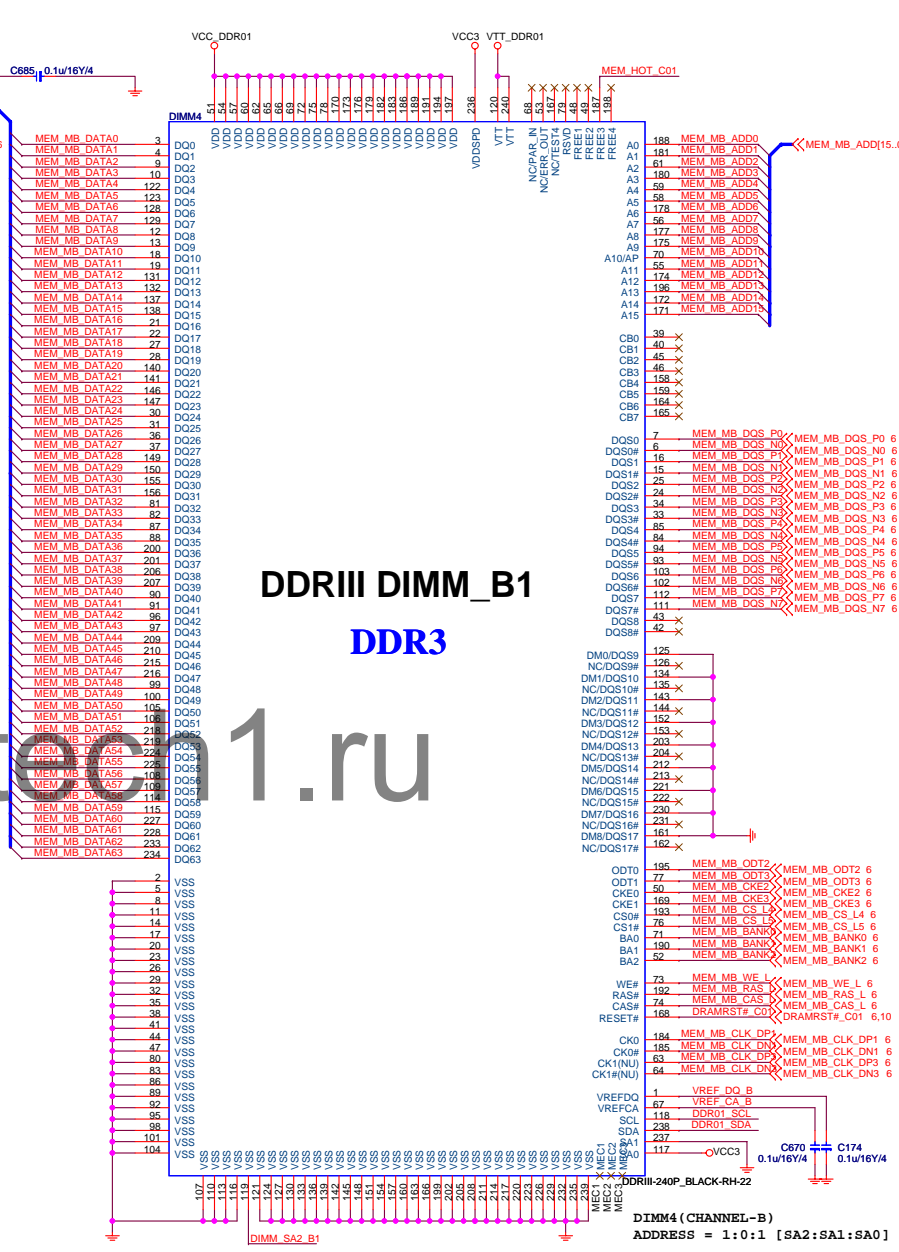
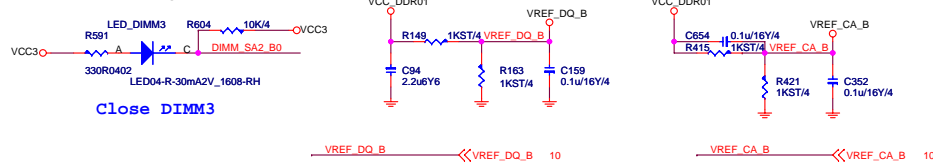
MS-7760

Size: Custom Document Description: **DDR3 Chane-A DIMM1/2** Rev: 1.1

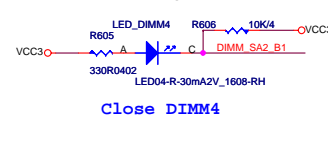
Date: Wednesday, October 12, 2011 Sheet: 10 of 54



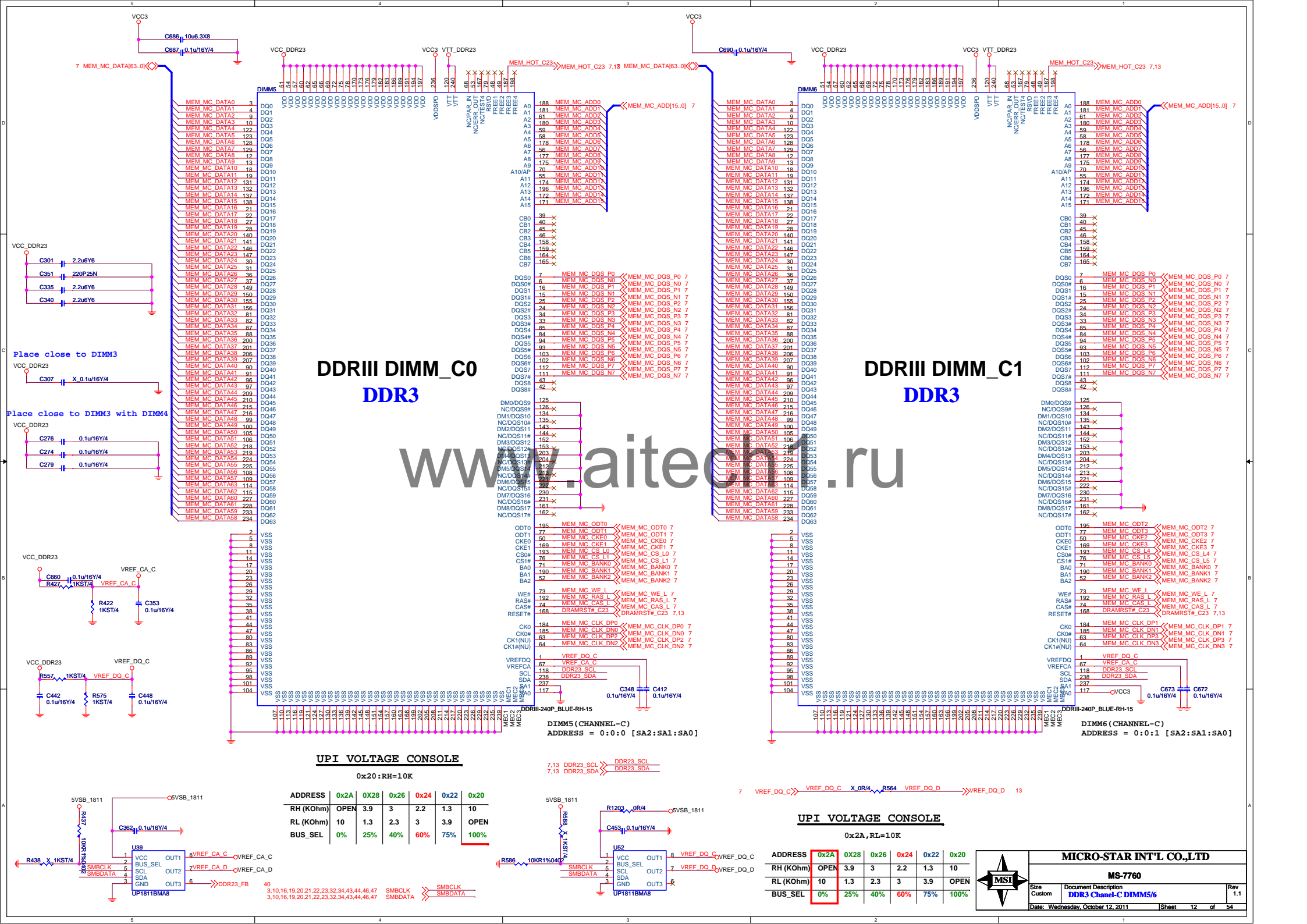
Warning LED

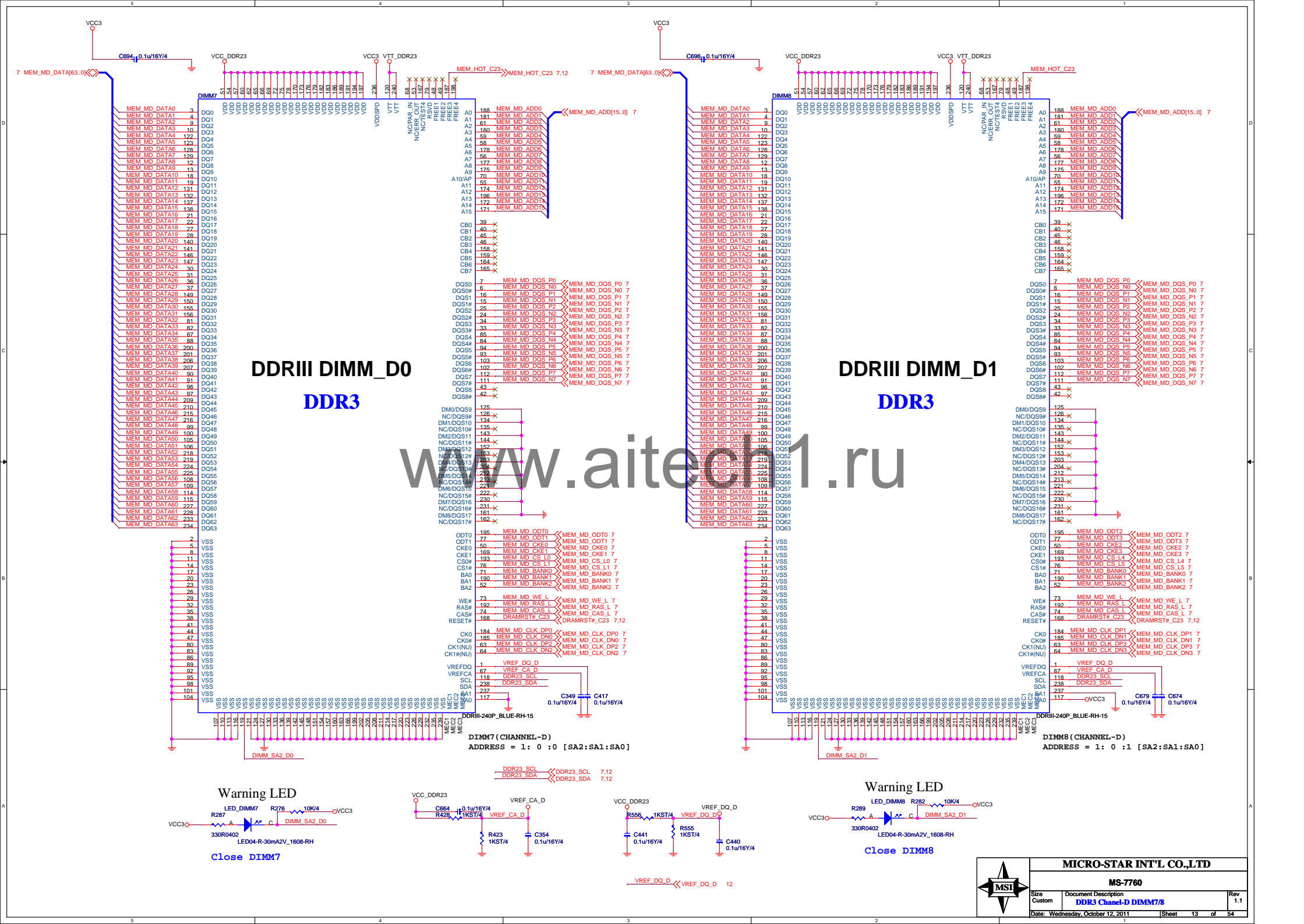


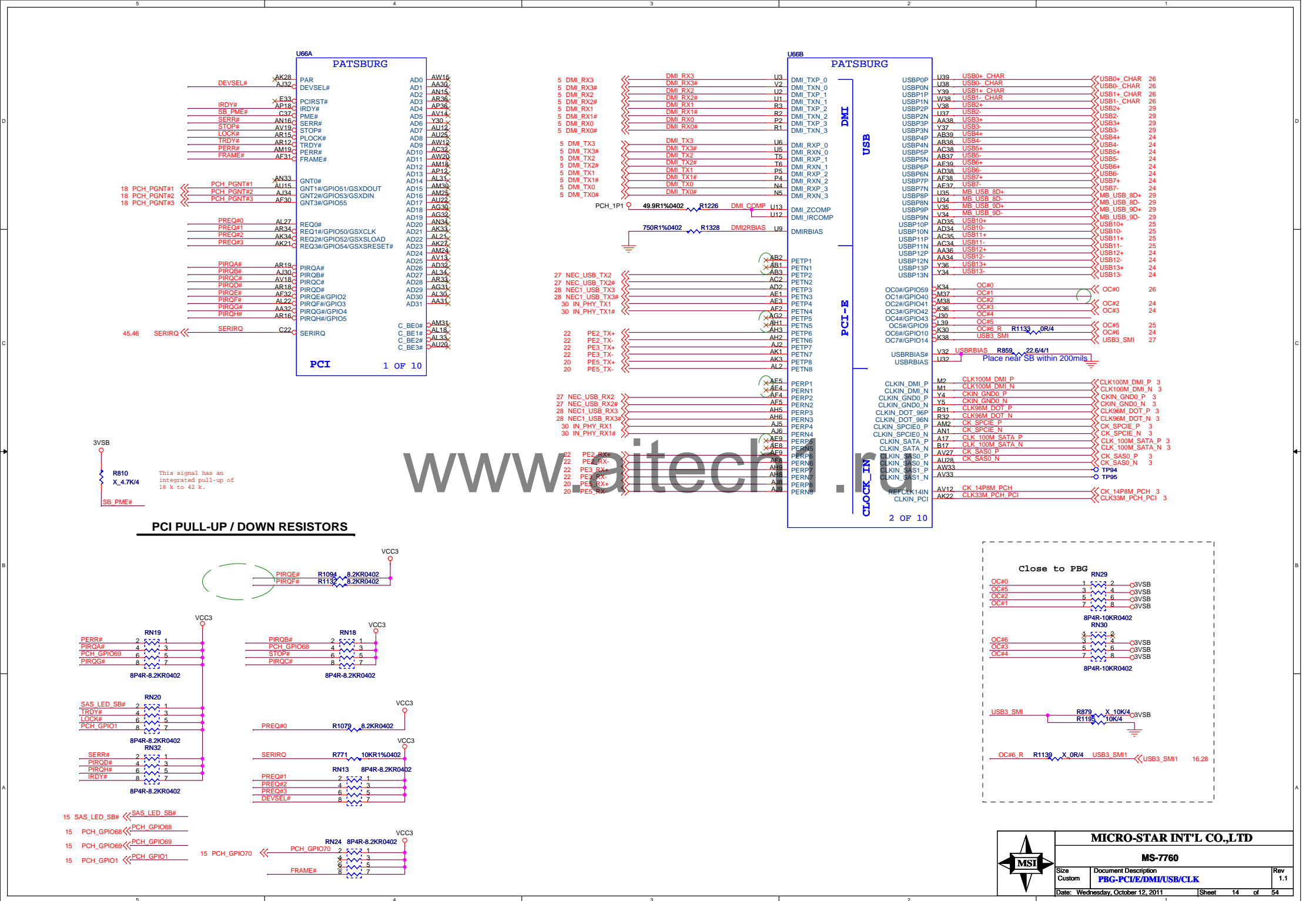
Warning LED

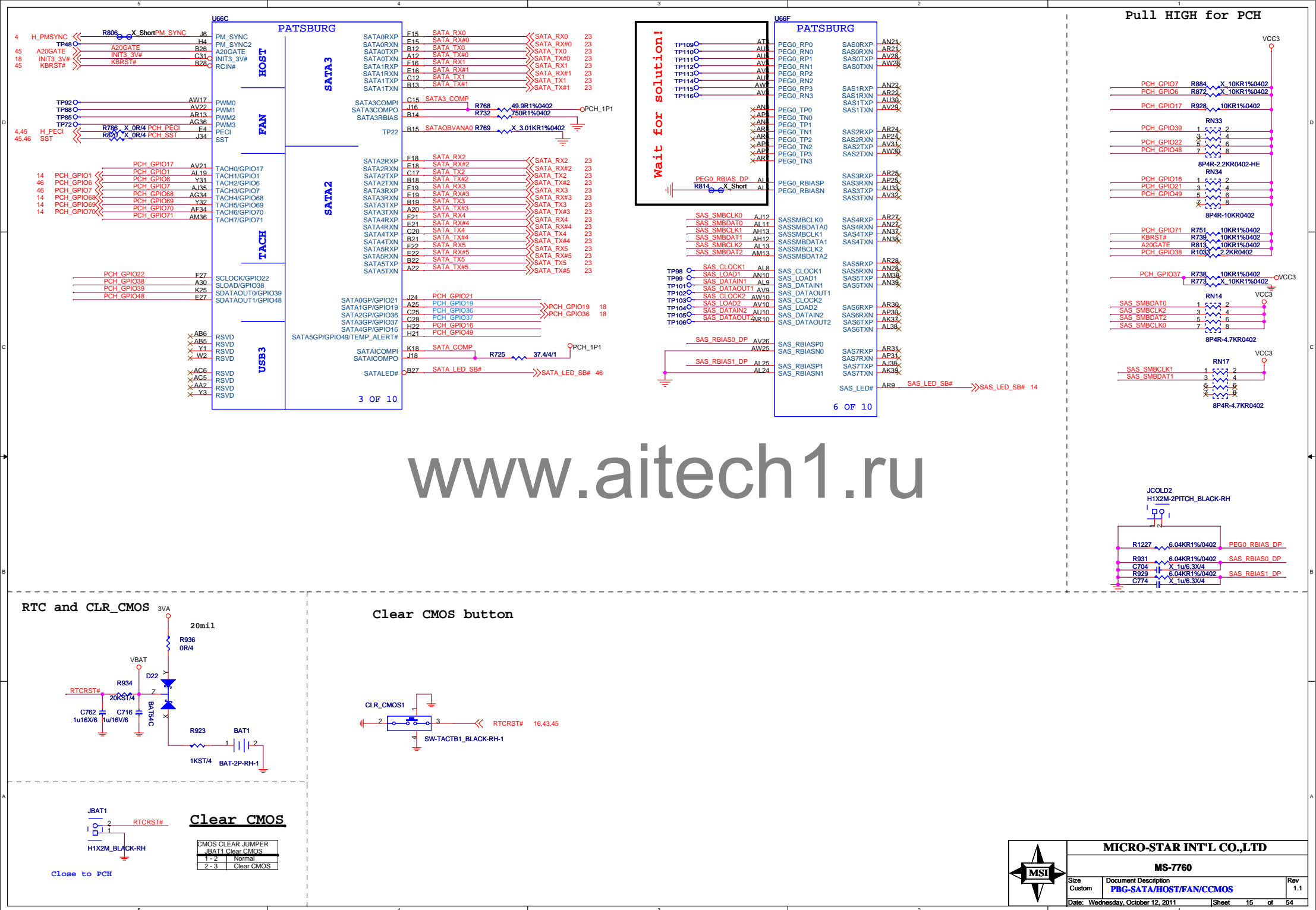


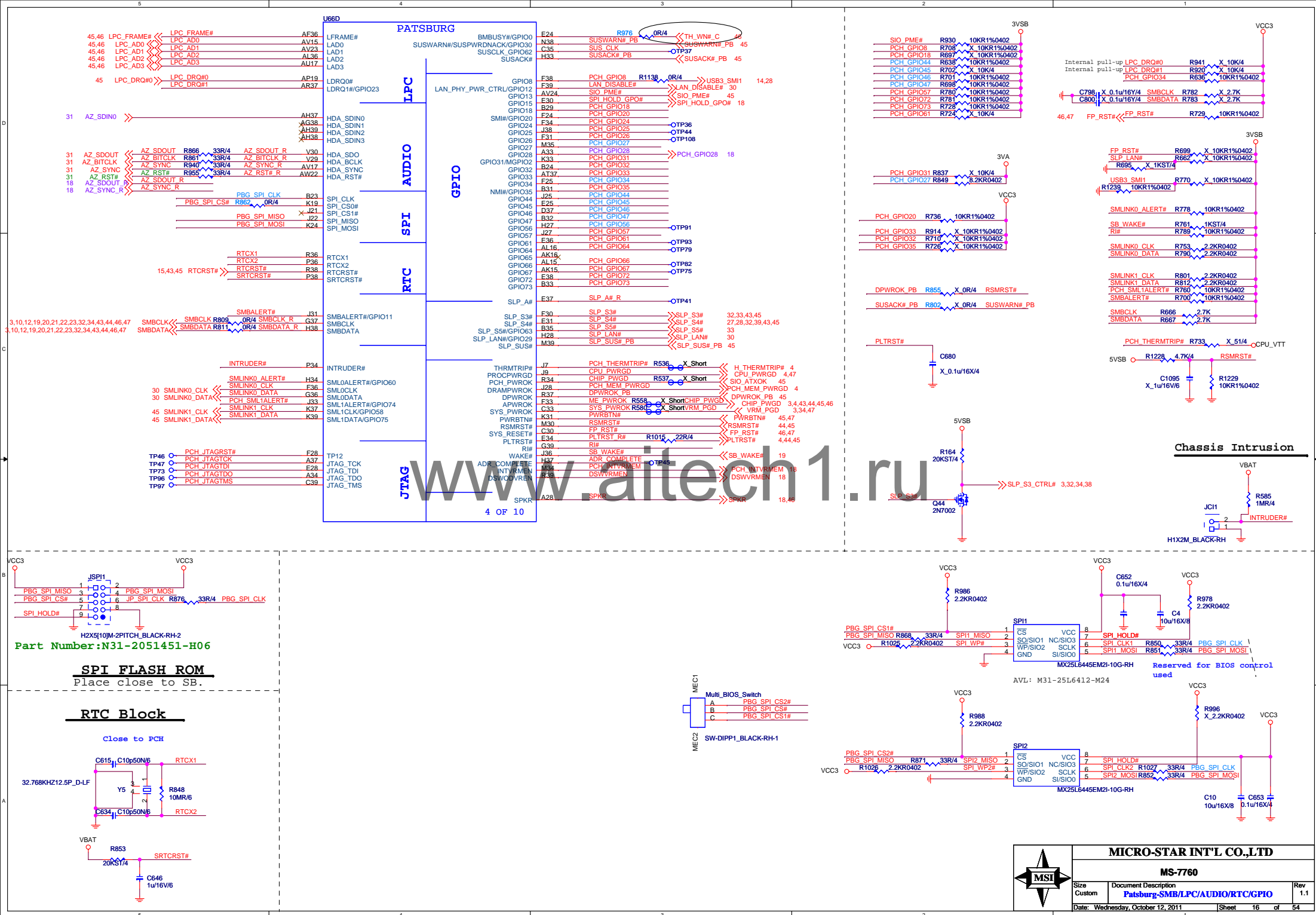
MICRO-STAR INT'L CO.,LTD			
MS-7760			
Size	Document Description	Rev	
Custom	DDR3 Chane-B DIMM3/4	1.1	
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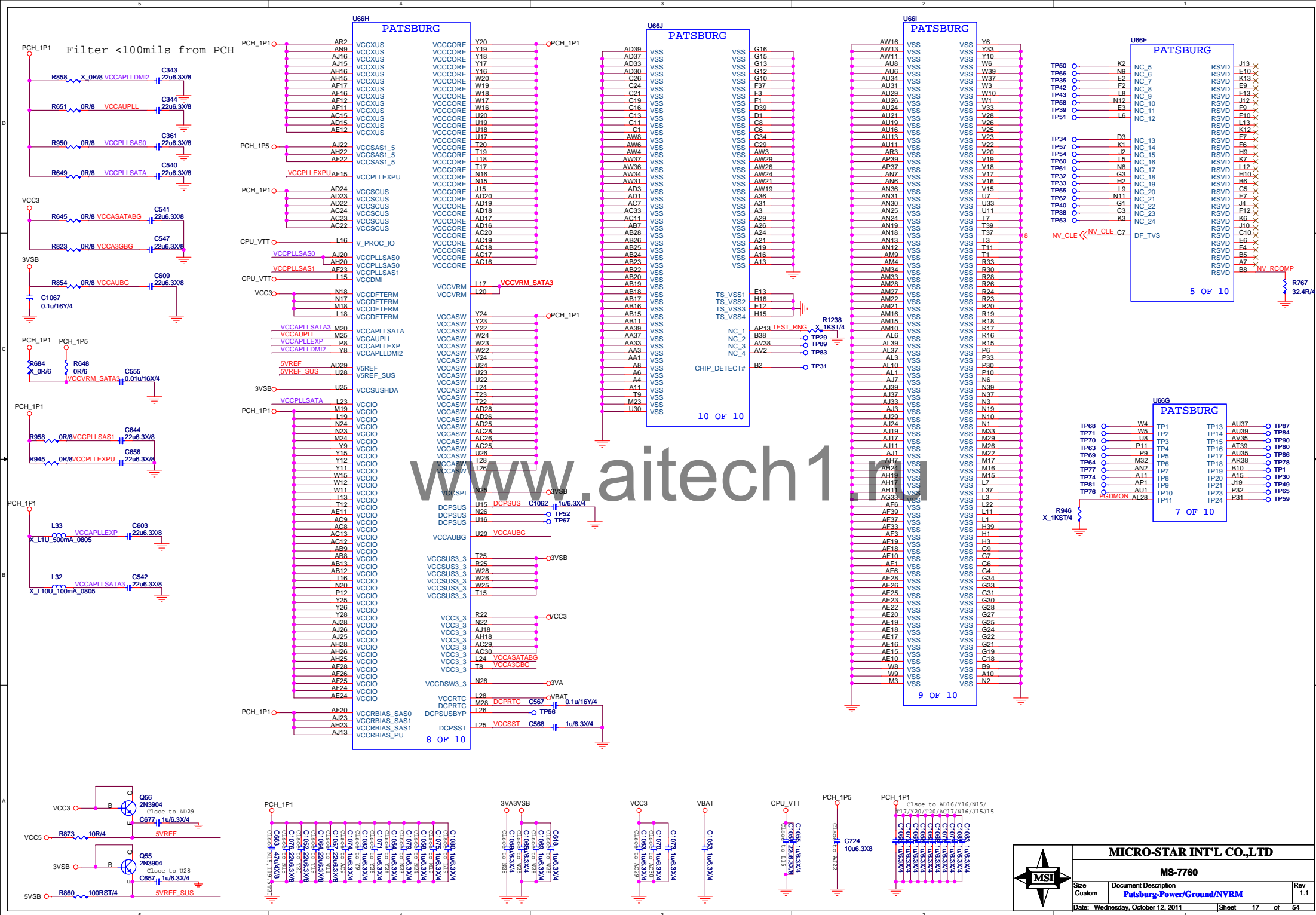






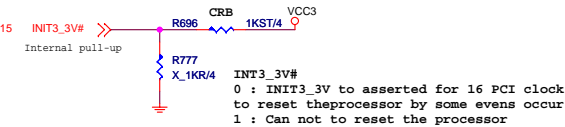
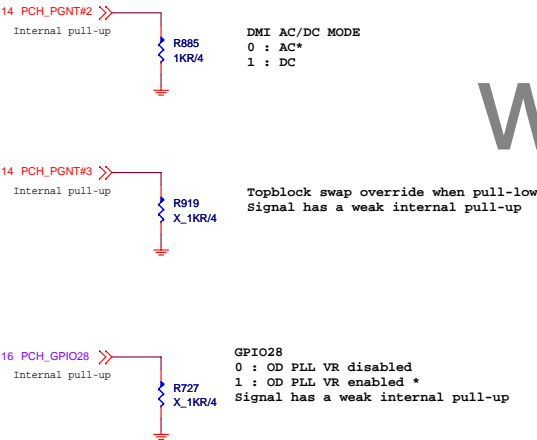
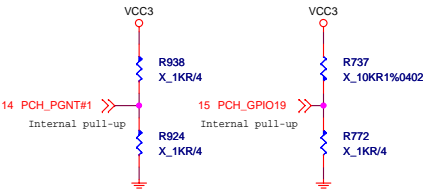






PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

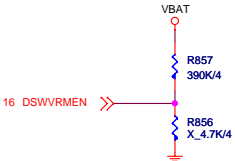


INTVRMEN

0 : DISABLE INTERNAL VRM

1 : ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

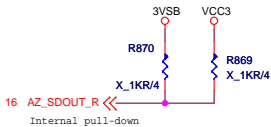


DSWVRMEN

0 : Disable Internal Deep Sleep 1.05 V regulators.

1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



HDA_SDO

Disable ME in Manufacturing Mode

when pull LOW ????

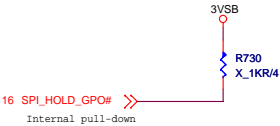


HDA_SYNC

OD PLL VR SUPPLY SEL

0: 1.8V SUPPLY

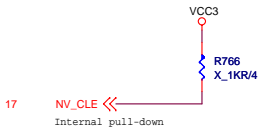
1: 1.5V SUPPLY *



GPIO15

0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *

1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

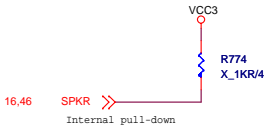


DMI/FDI TERMINATION VOLTAGE

DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH

DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?

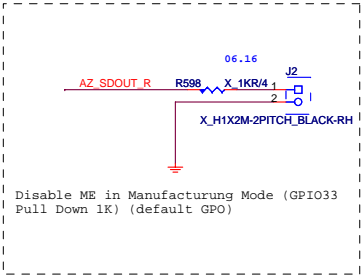
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



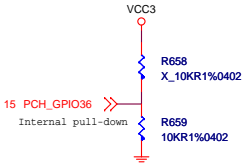
SPKR

0 : EN TCO REBOOT *

1 : DIS TCO REBOOT



Disable ME in Manufacturing Mode (GPIO33 Pull Down 1K) (default GPO)



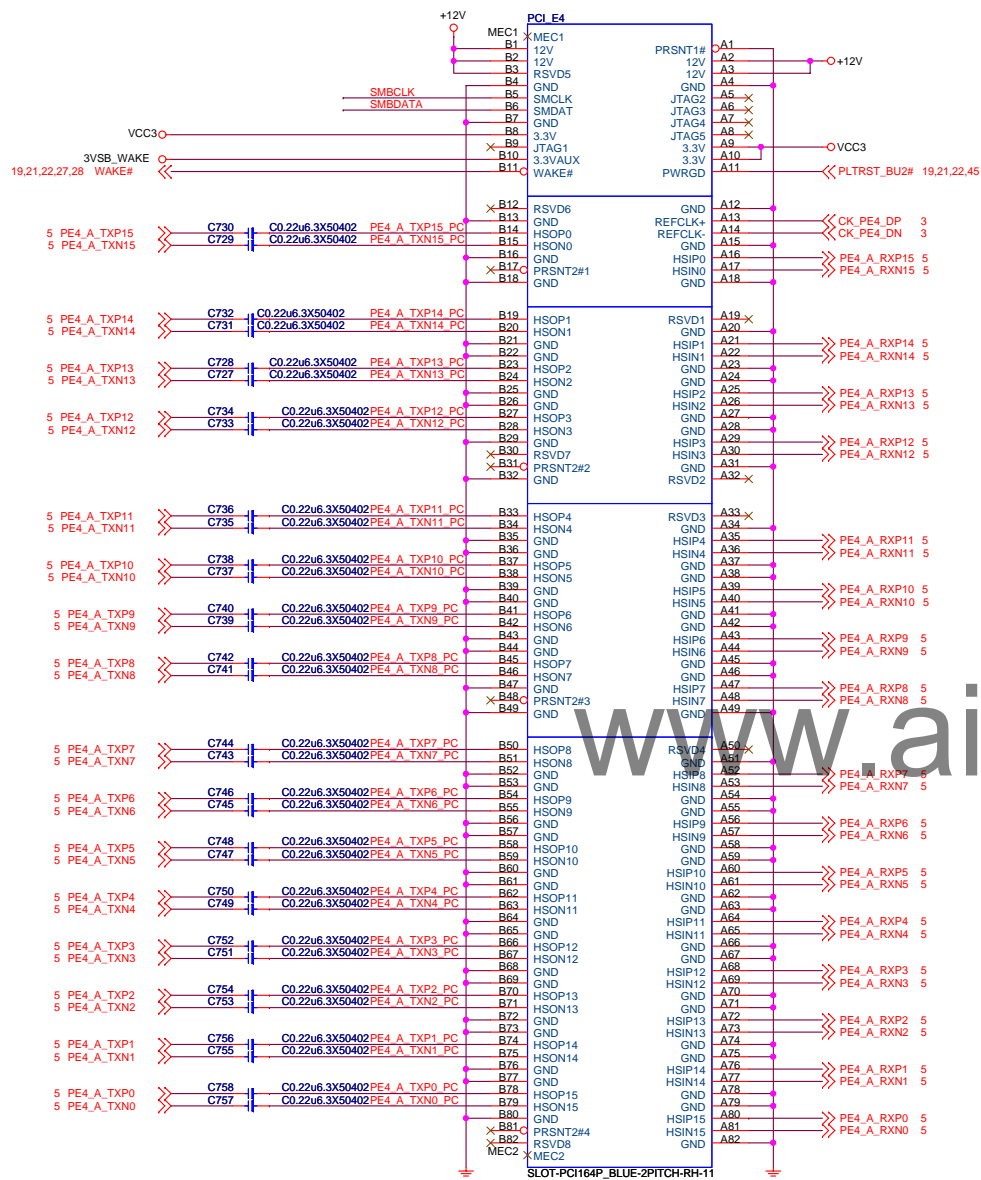
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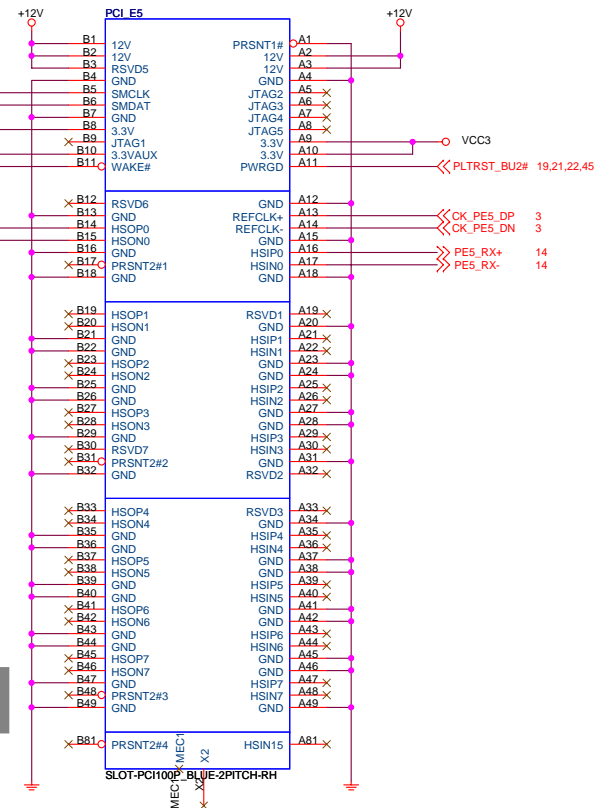
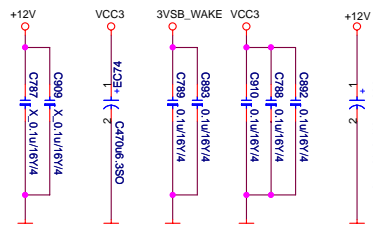
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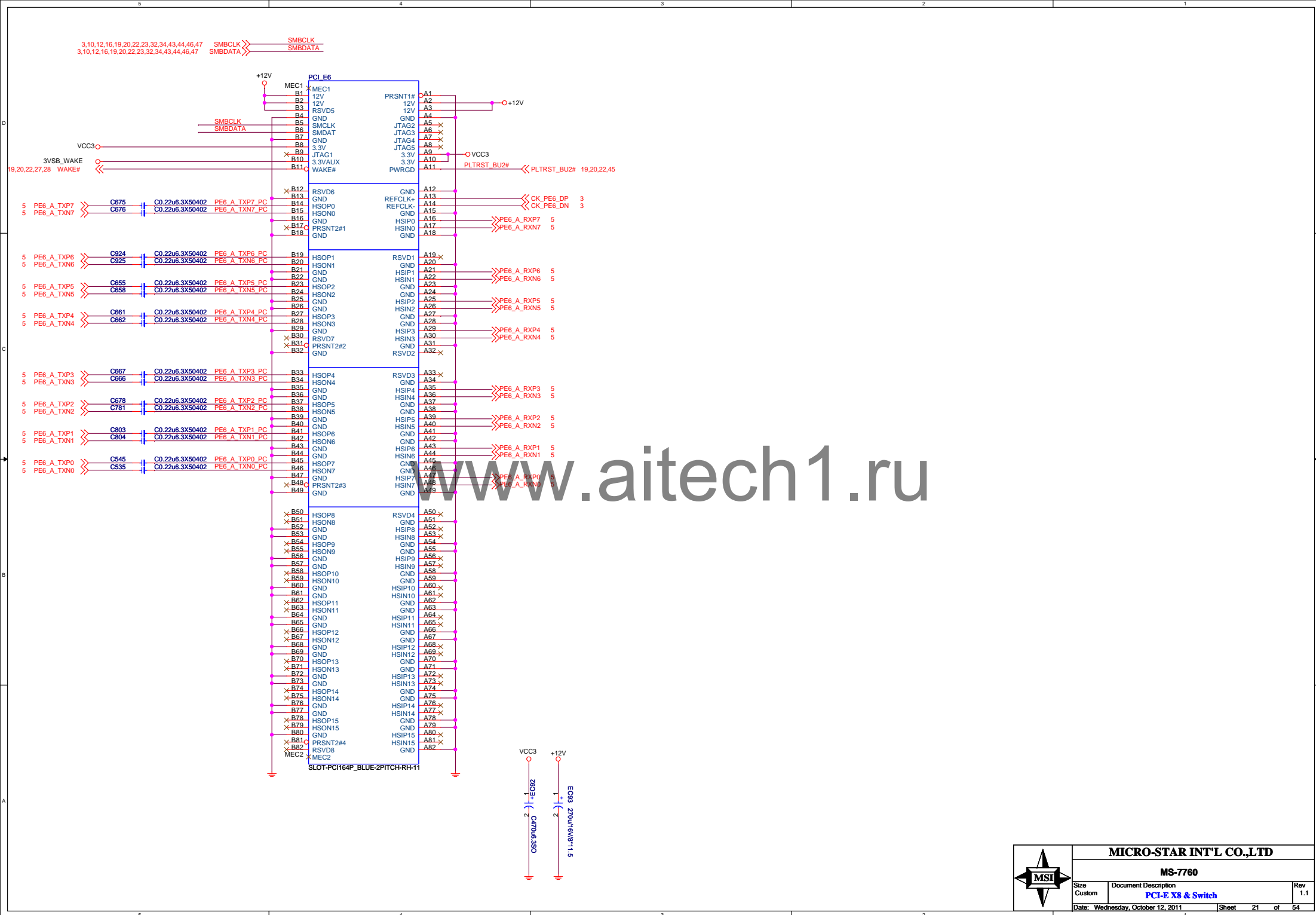
3,10,12,16,19,21,22,23,32,34,43,44,46,47
3,10,12,16,19,21,22,23,32,34,43,44,46,47

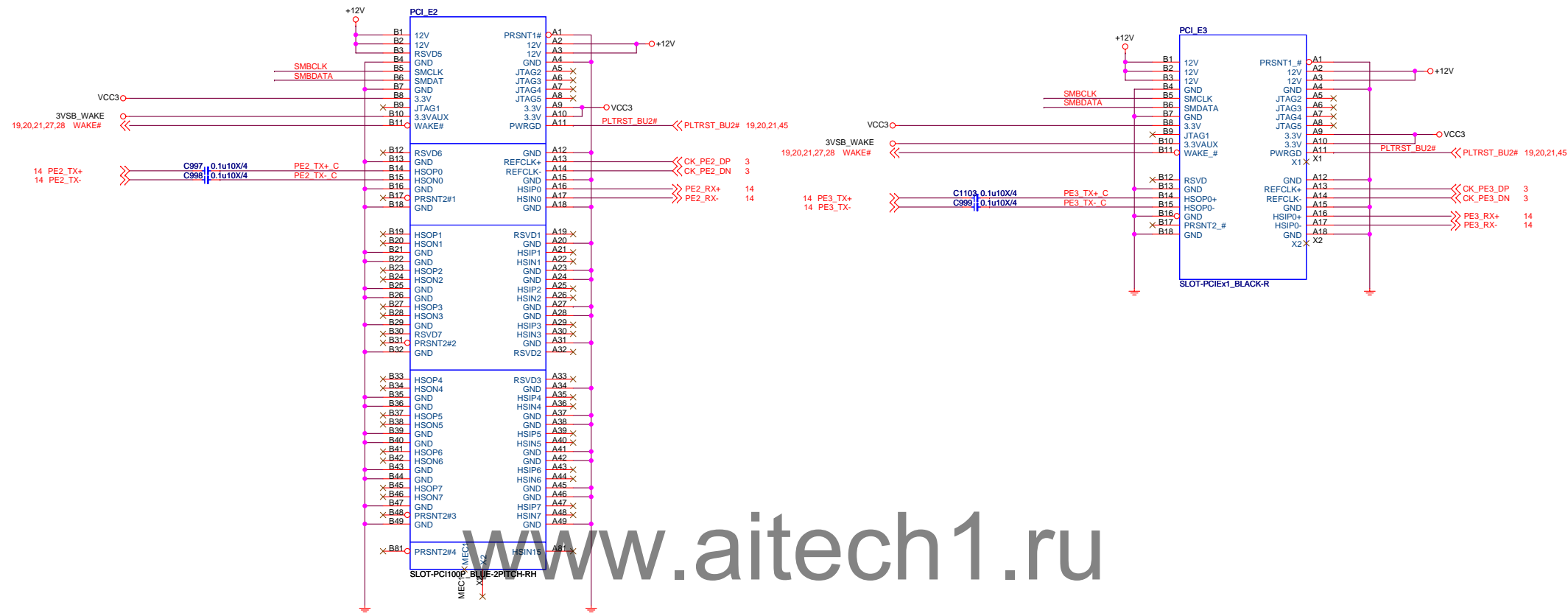
SMBCLK
SMBDATA



within 500mil

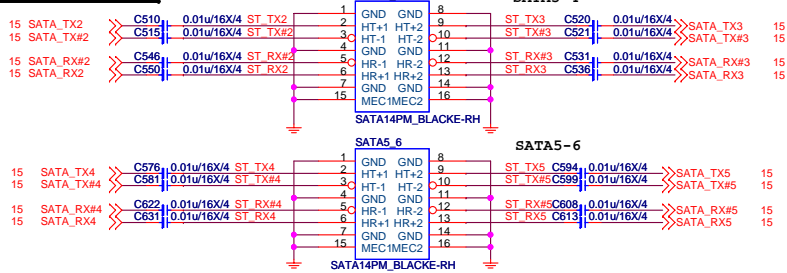




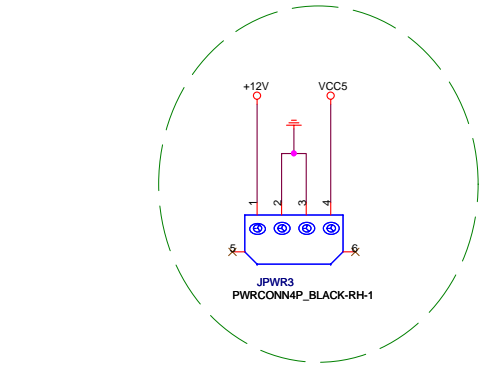
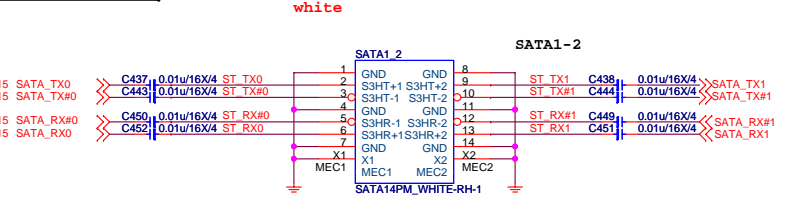


3,10,12,16,19,20,21,23,32,34,43,44,46,47 SMBCLK SMBCLK
3,10,12,16,19,20,21,23,32,34,43,44,46,47 SMBDATA SMBDATA

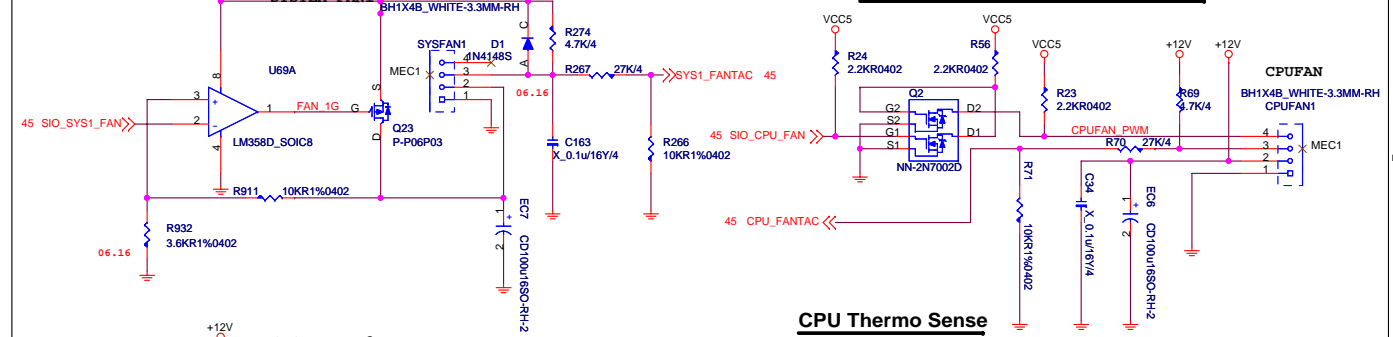
SATA2 Ports



SATA3 Ports



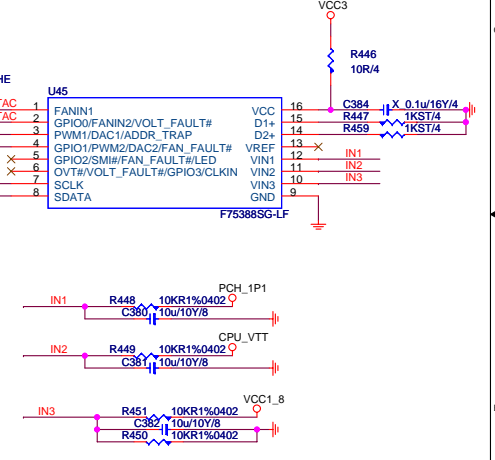
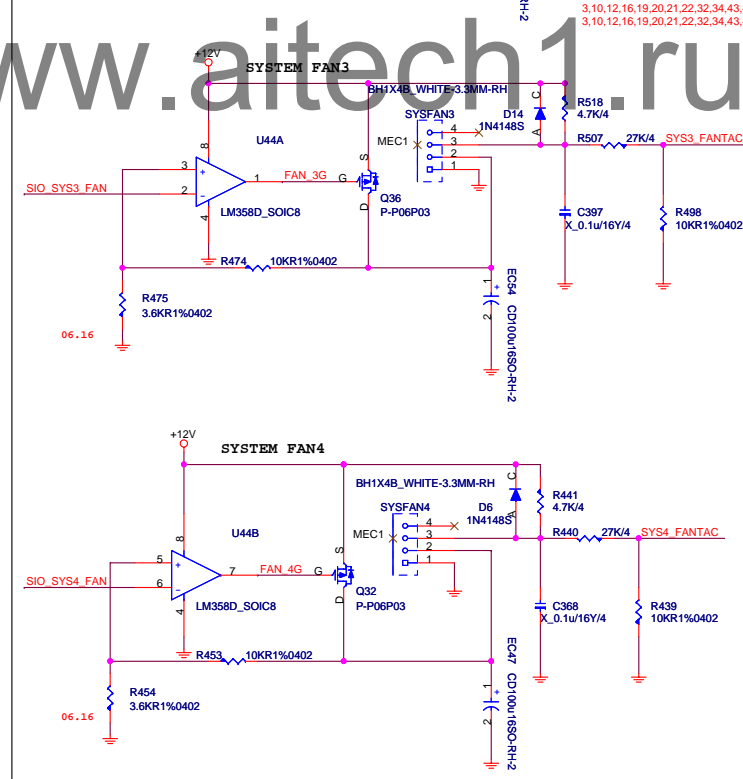
CPU FAN-COUNTROL CIRCUIT



CPU Thermo Sense

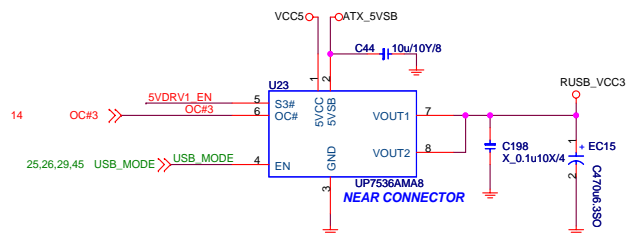
FAN initial Speed setting(PIN3)

FAN Speed rate	I2C Address	FAN Type	R324
60%	0x5A	DAC	NC
100%	0x5C	DAC	200K
60%	0x5C	PWM	*16K
100%	0x5A	PWM	2.2K

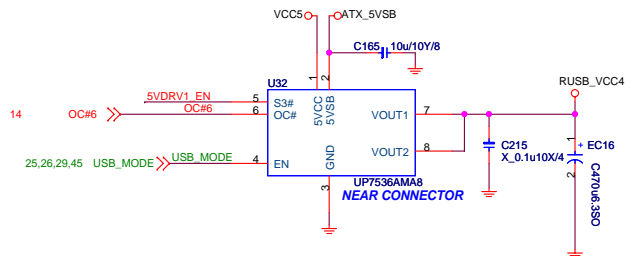


HW Monitor

USB POWER FOR PORT 6,7

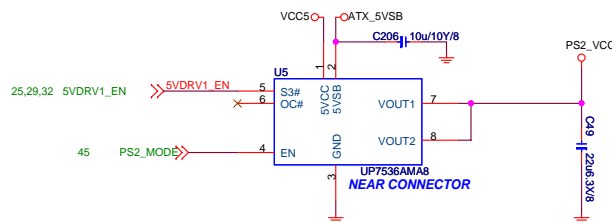


USB POWER FOR PORT 12,13

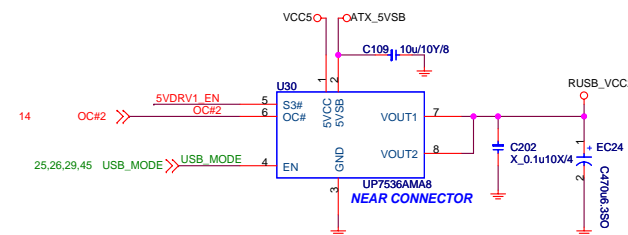


Rear USB Connector

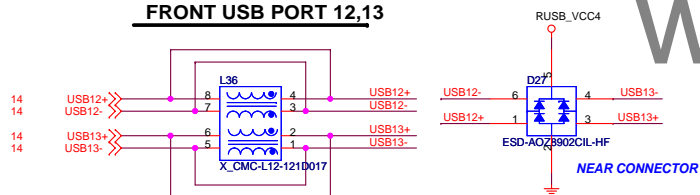
PS2 POWER



USB POWER FOR PORT 4,5

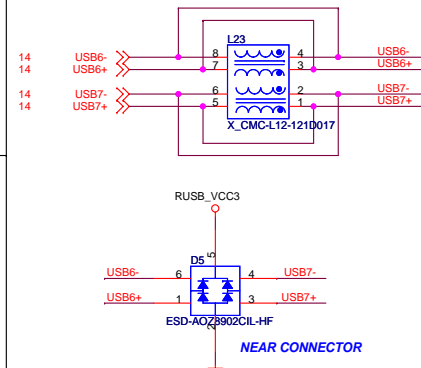


FRONT USB PORT 12,13

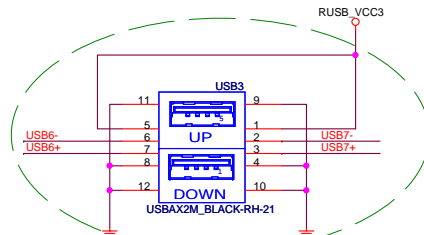
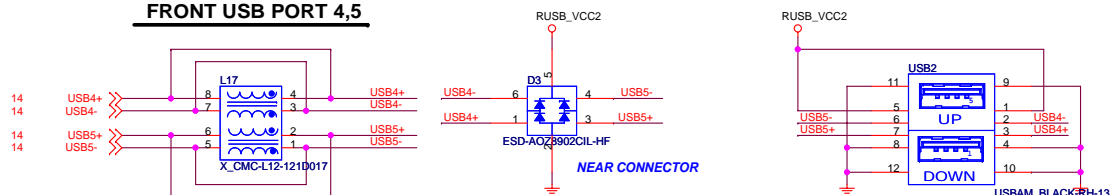


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FRONT USB PORT 6,7



FRONT USB PORT 4,5

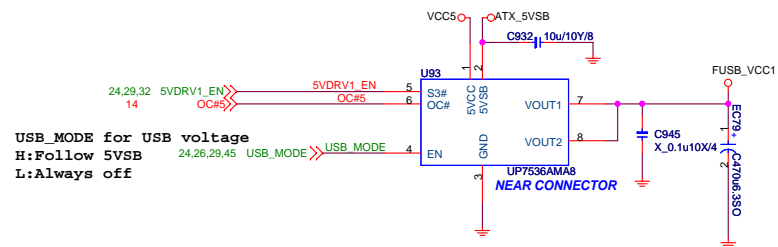


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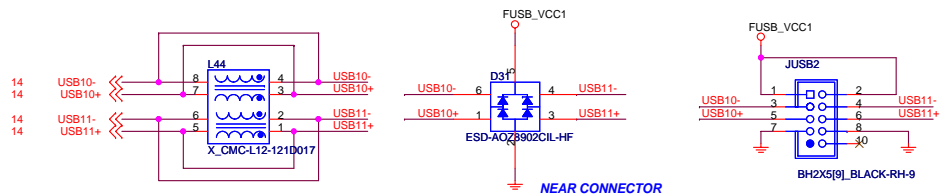
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USB POWER FOR 10,11



FRONT USB PORT 10,11



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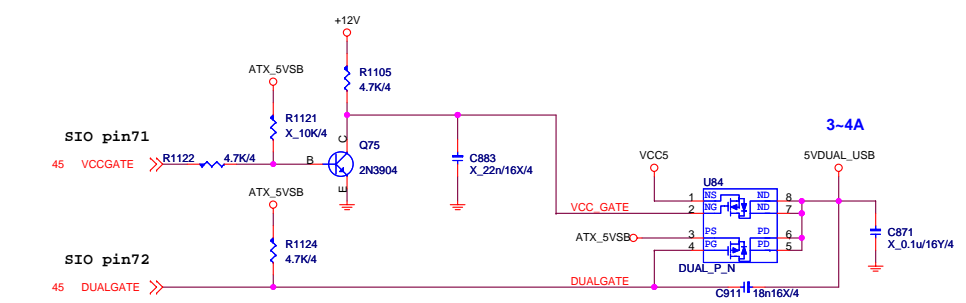


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MS-7760

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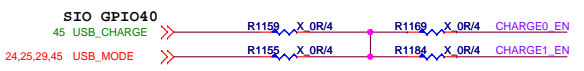
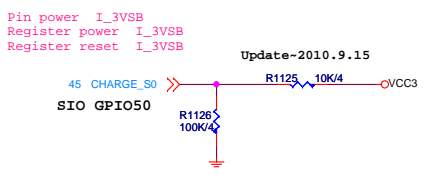
5VDUAL_USB



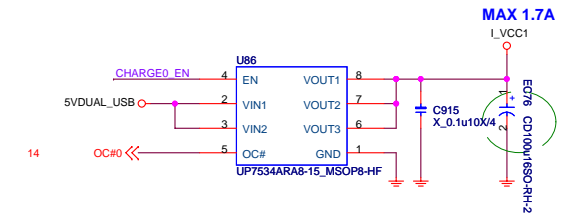
SIO GPIO40 Pin7 (I_VSB3V)
USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

Pin power I_3VSB or VBAT
Register power I_3VSB or VBAT
Register reset I_3VSB or VBAT

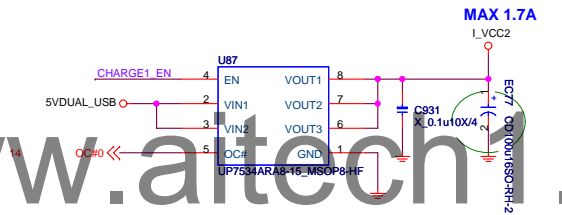
Power plug in , H/W default support USB charge.



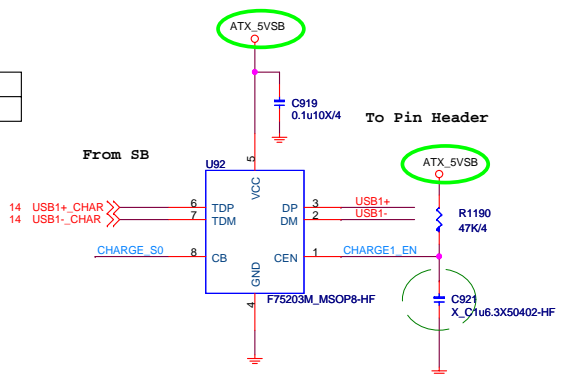
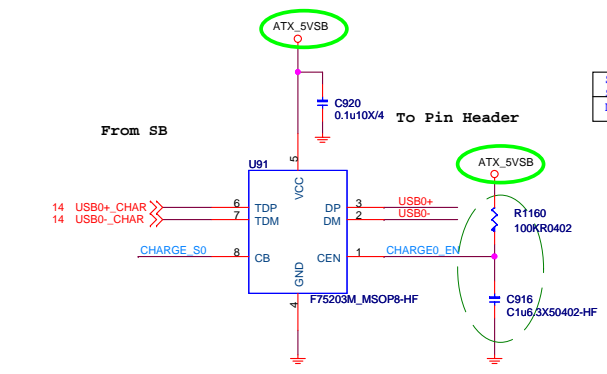
USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging

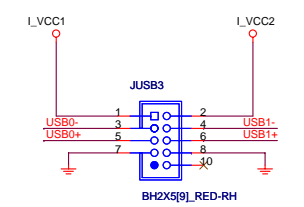
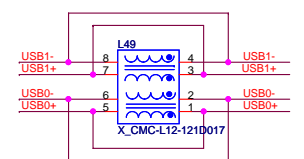


** If your spec will not need bom option, please don't co-lay blue labels.



A type
2.70V< D+ <3.1 V
1.85V< D- < 2.1V
For i-Pad / i-Phone 4G charges current up to 1.6A.

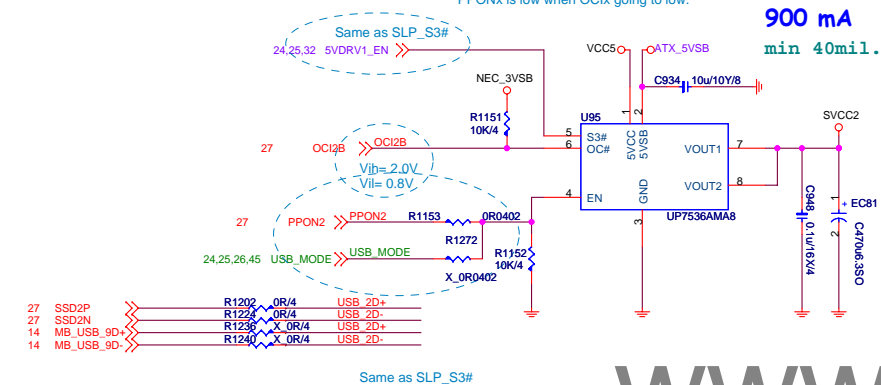
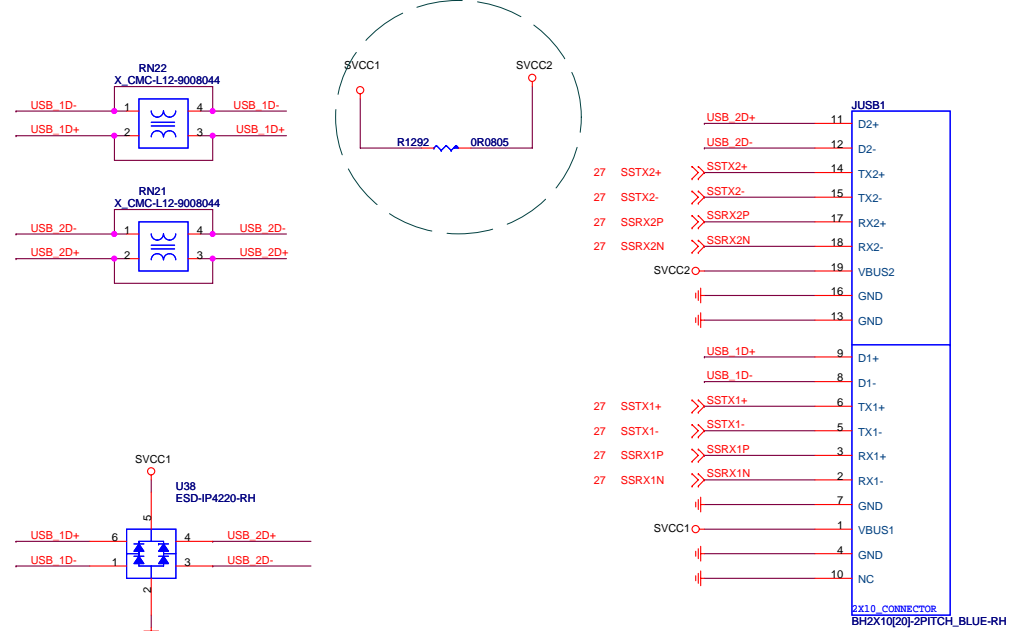
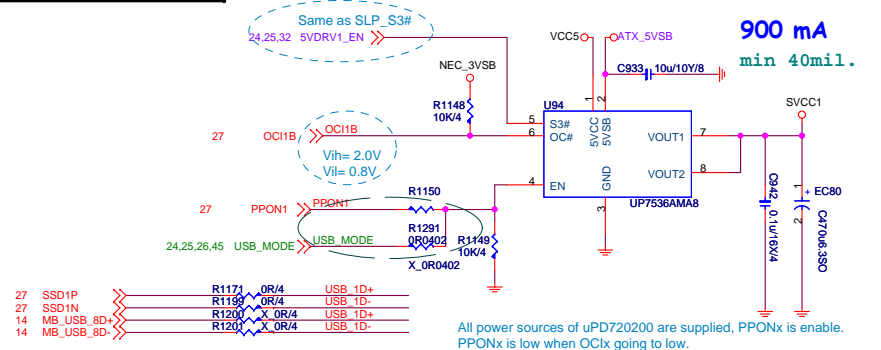
FRONT USB PORT 0,1



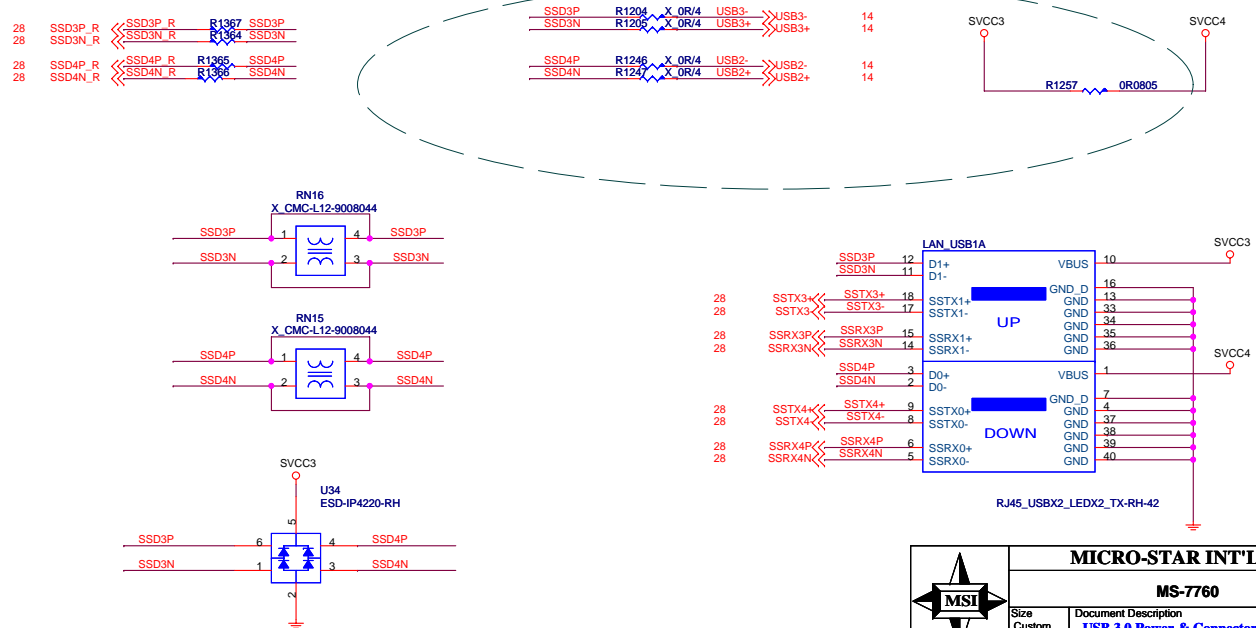
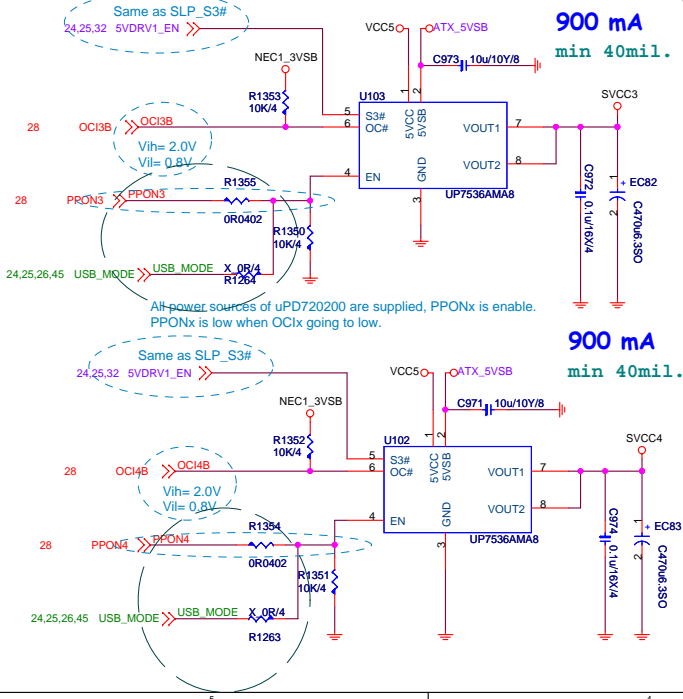
Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

PI5USB14550 has internal EDS diode.

FRONT USB PORT 8,9



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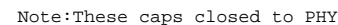


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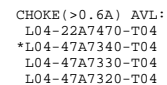
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If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,
the CLK_REQ_N pull-up resistor should be connected
to +V3.3s



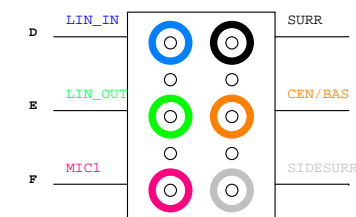
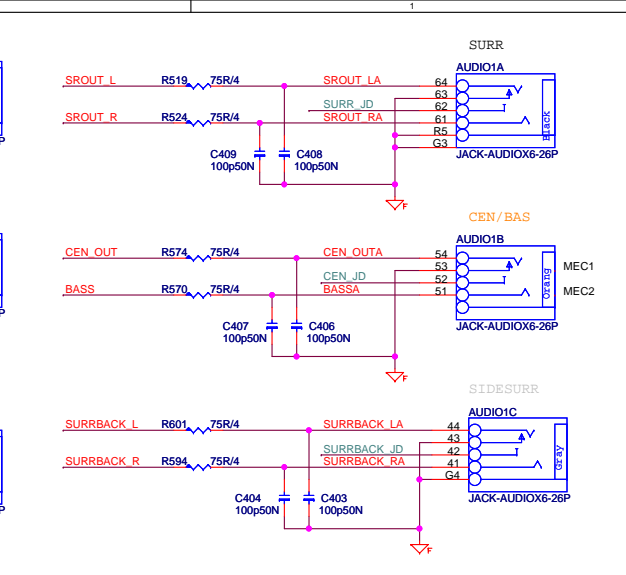
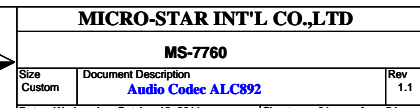
LAN Connector



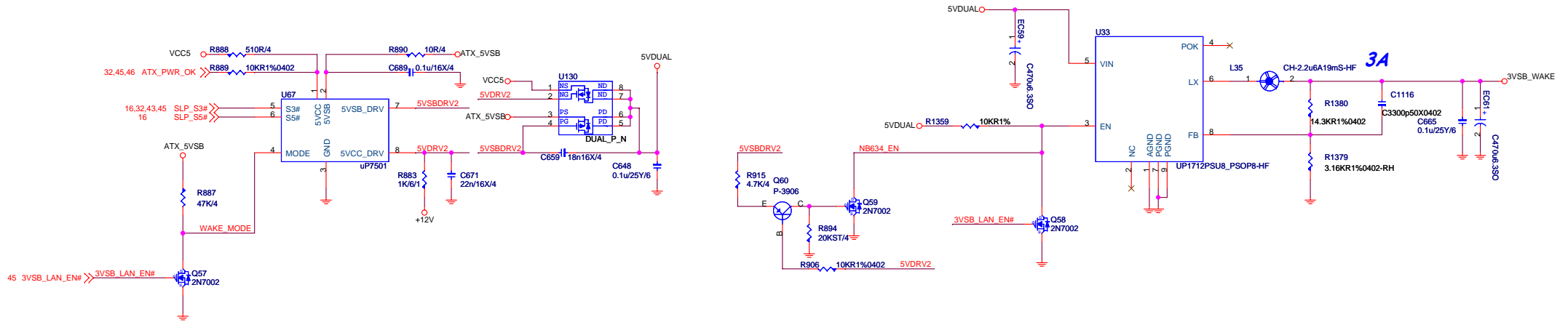
MS-7760

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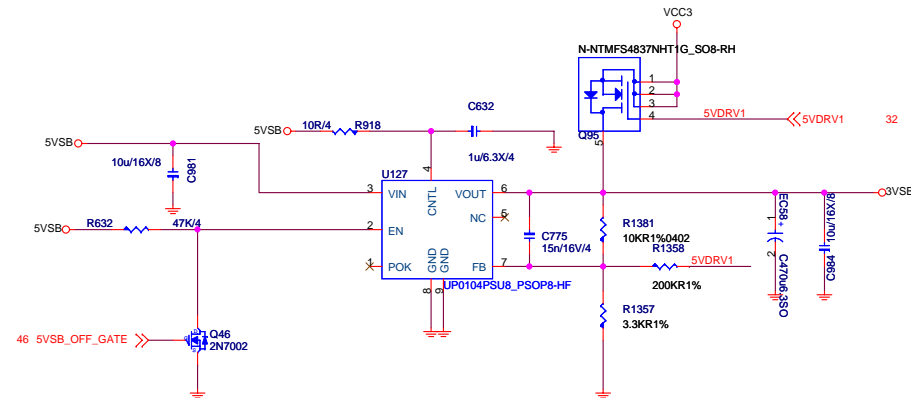
[illegible]

3VSB_WAKE

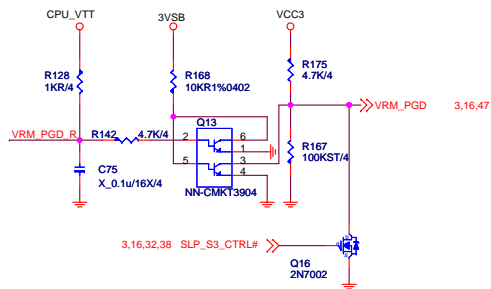


3VSB

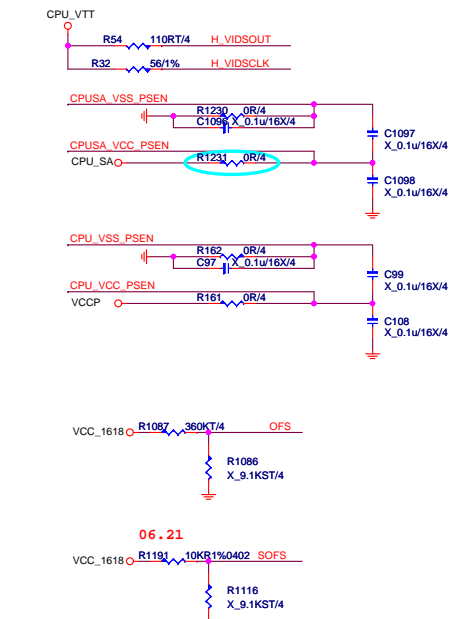
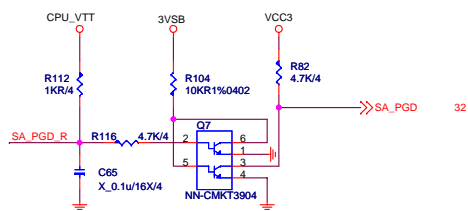
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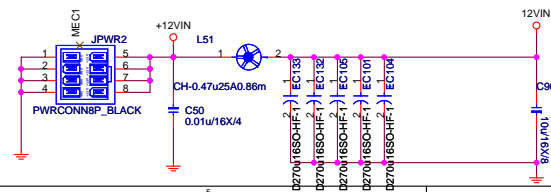
VRMPWRGD LEVEL SHIFT



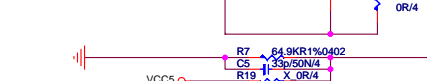
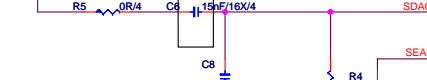
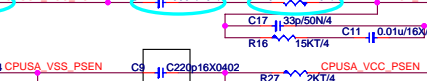
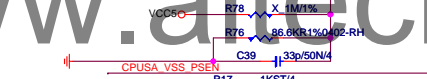
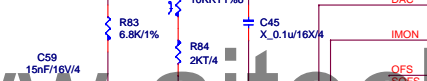
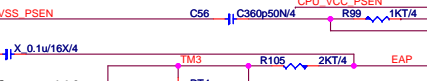
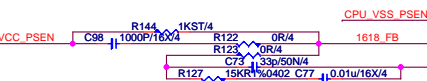
SAPGD LEVEL SHIFT



$$5000\text{mA} \times 4 \times 1 = 20\text{A} > 13.7\text{A} \quad (7.68)$$



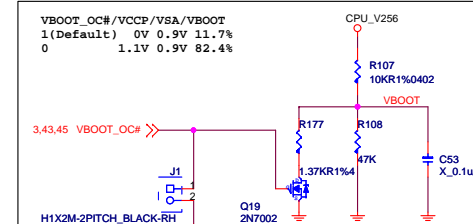
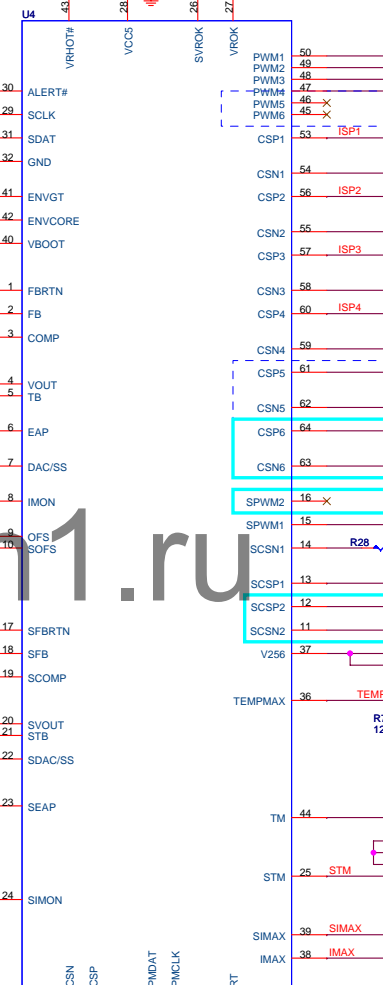
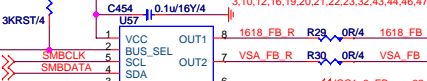
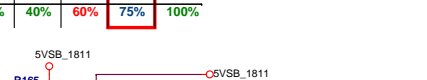
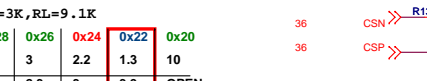
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND

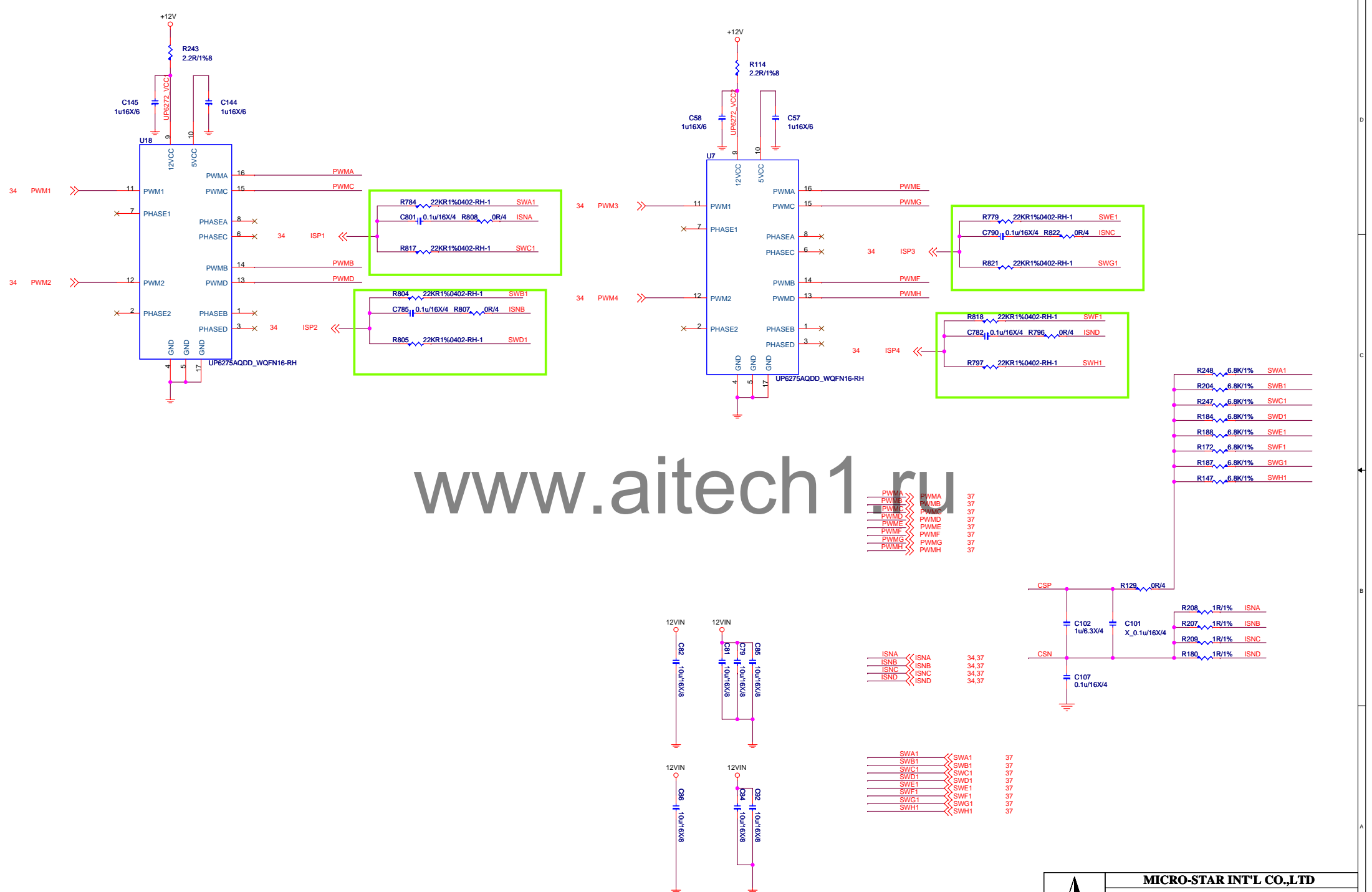


UPI VOLTAGE CONSOLE

0x22: RH=3K, RL=9.1K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%





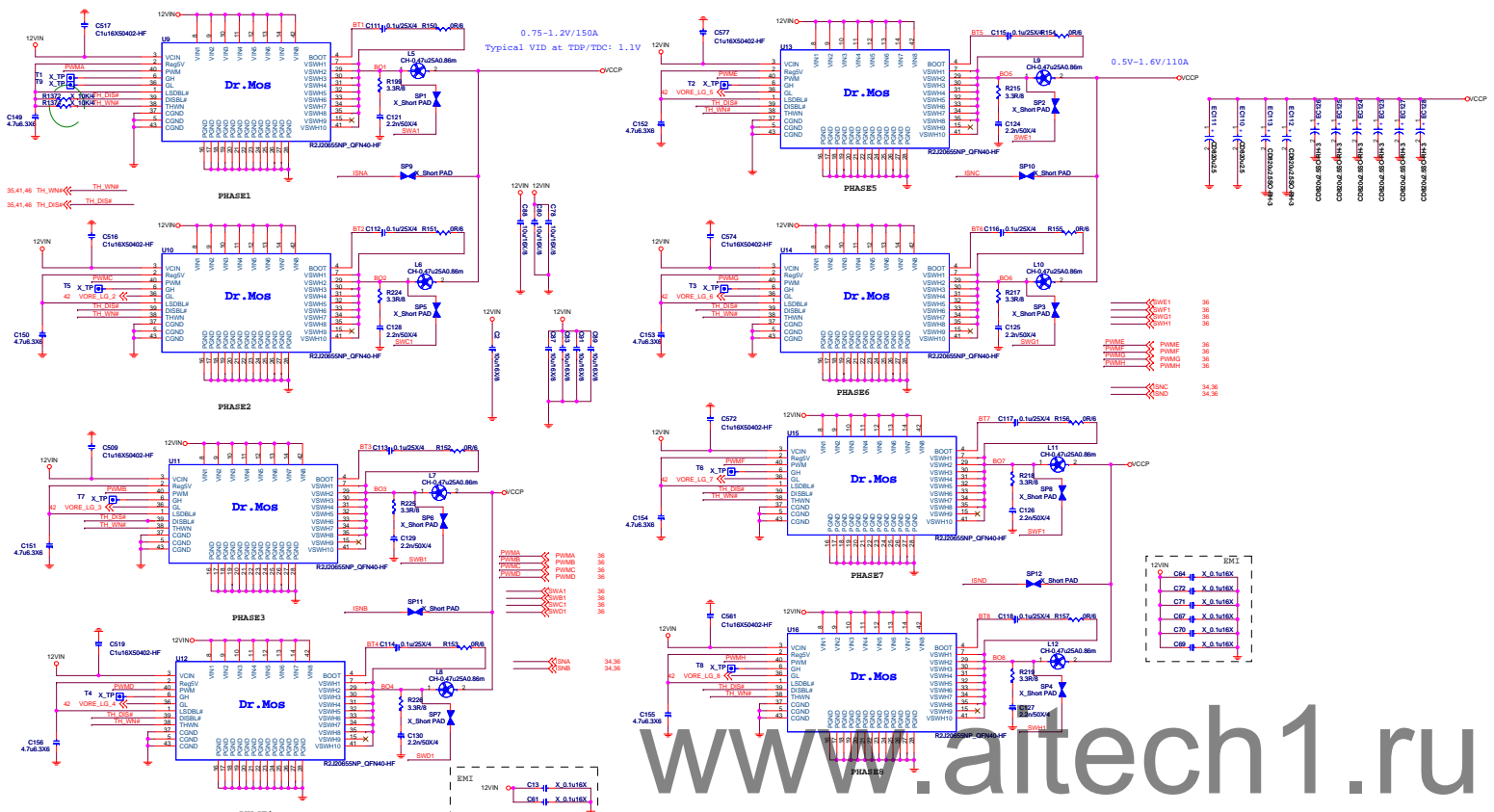
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- PWMA 37
- PWMB 37
- PWMC 37
- PWMD 37
- PWME 37
- PWMF 37
- PWMG 37
- PWMH 37

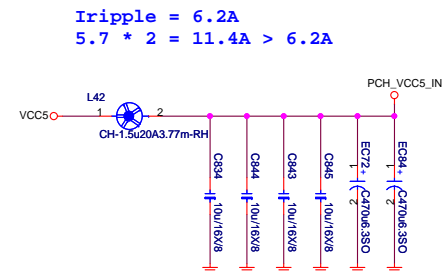
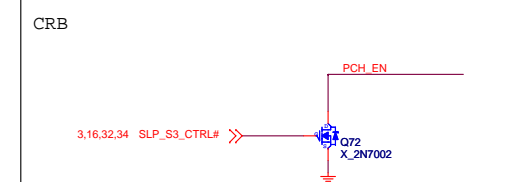
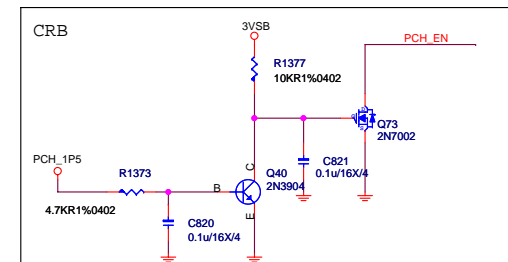
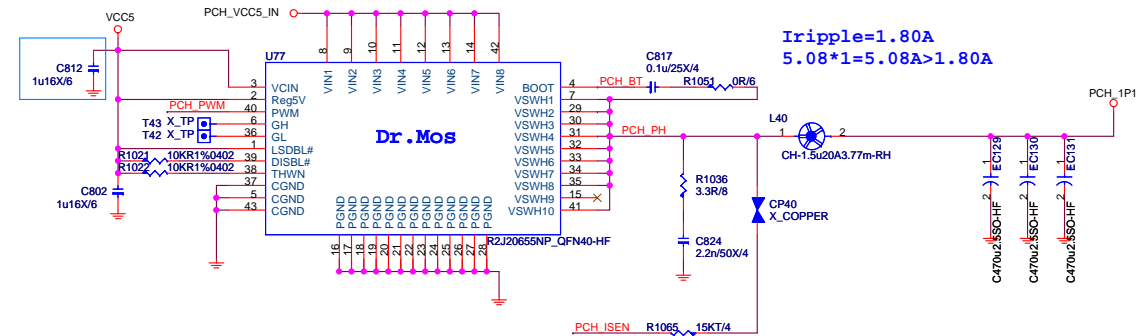
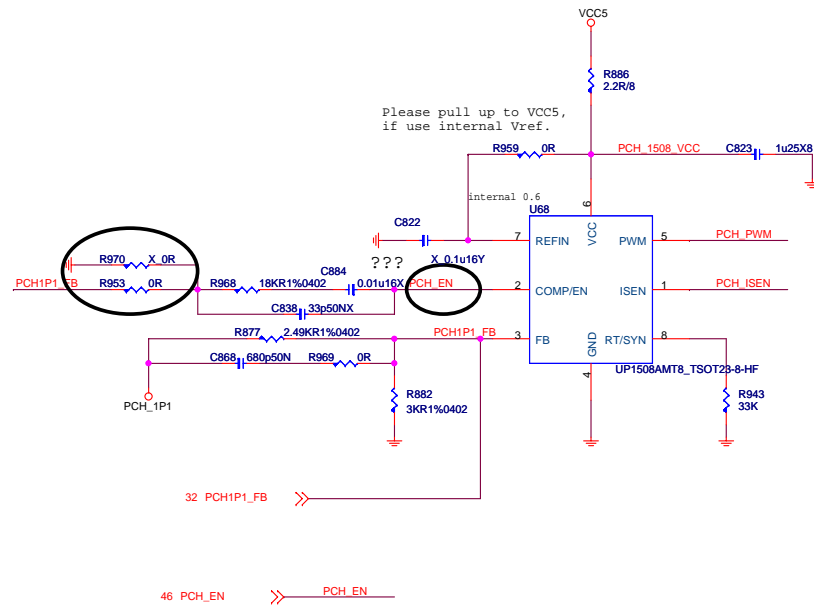
- ISNA 34,37
- ISNB 34,37
- ISNC 34,37
- ISND 34,37

- SWA1 37
- SWB1 37
- SWC1 37
- SWD1 37
- SWF1 37
- SWG1 37
- SWH1 37

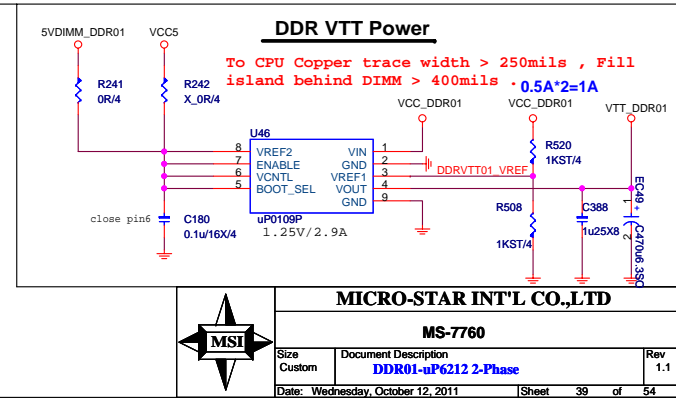
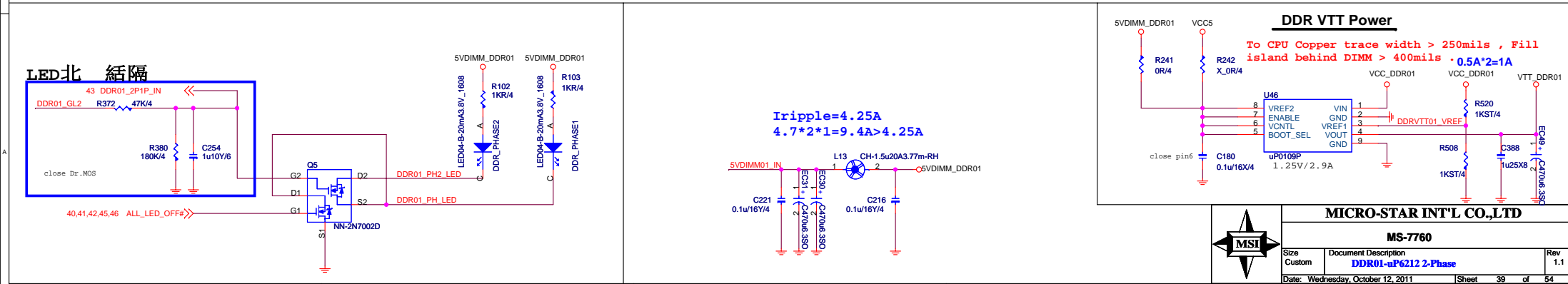
- CSP 34
- CSN 34



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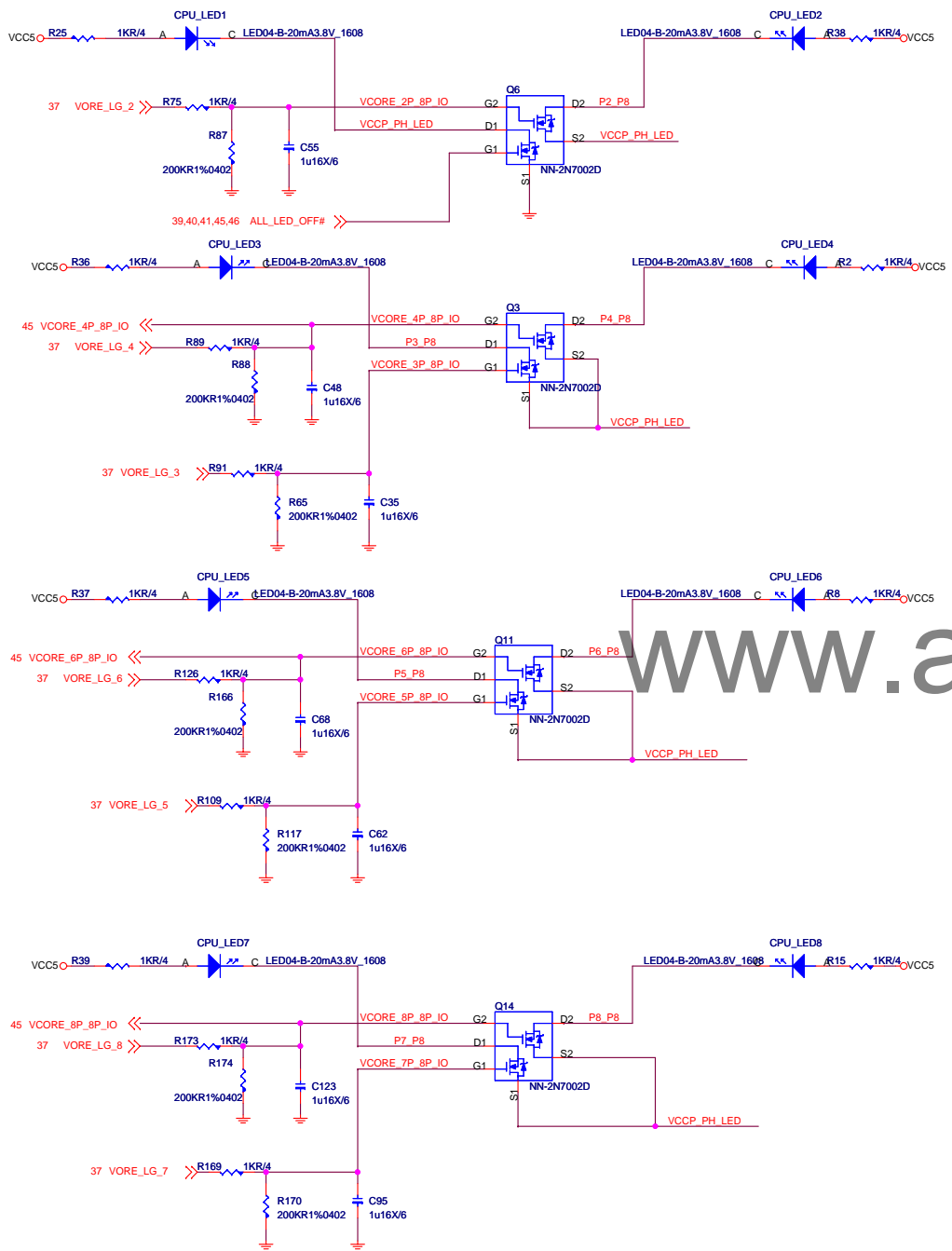
DDR3 1.5V 20A



D

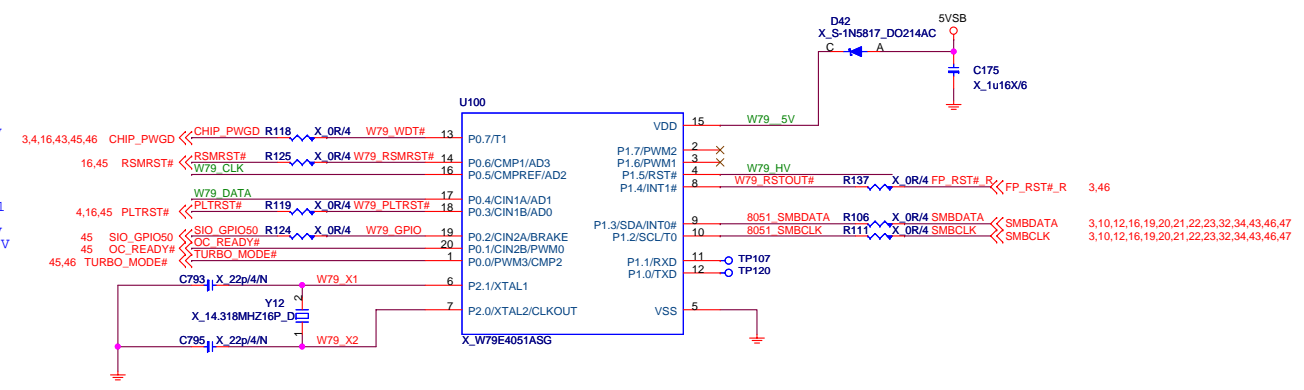






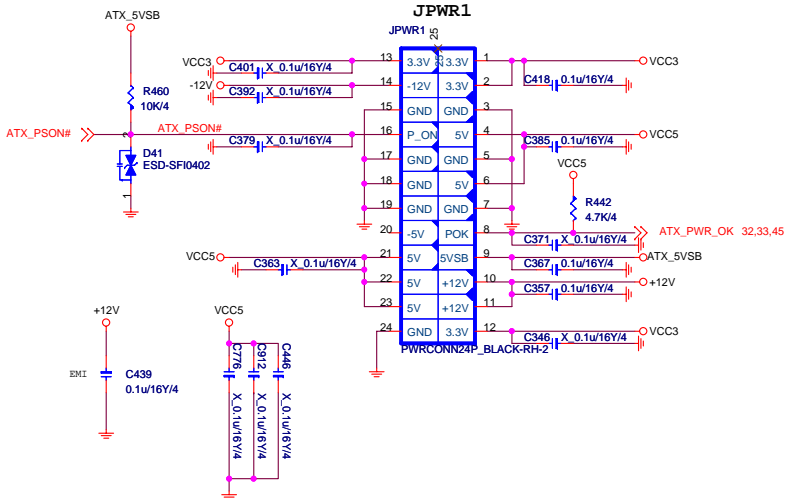
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out for Full reset, can pull up to 3V
RSMRST# for 8051 refer to read GPIO state
ICP Programmer
ICP Programmer
PLTRST# is a power on event for 8051
Reserved, can pull to 3V
BIOS inform to 8051 the OC ready, can pull up to 3V
OC Button, can pull up to 3V

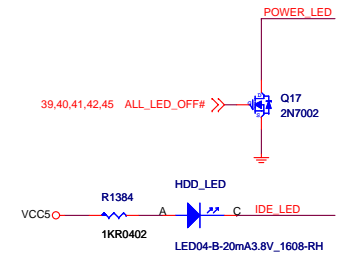
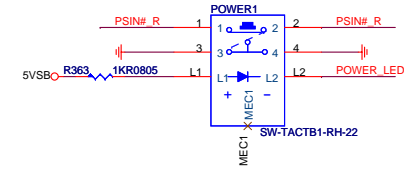
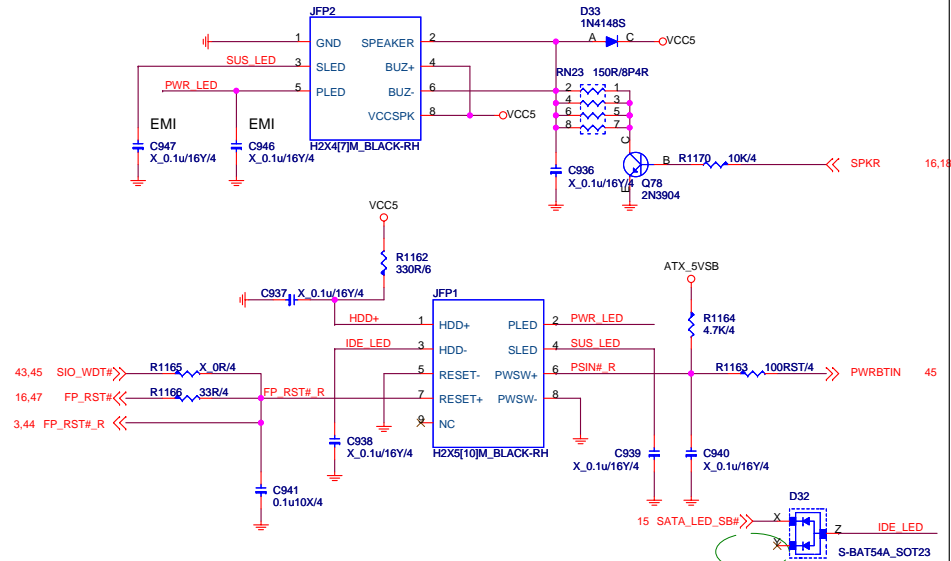


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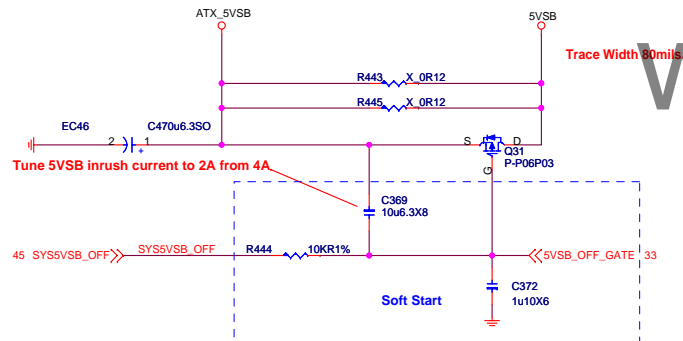
ATX POWER CONNECTOR



FRONT PANNEL

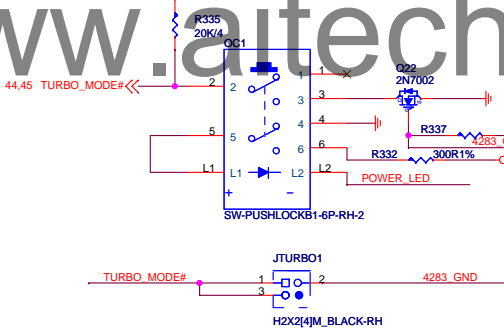


5VSB Power Switch



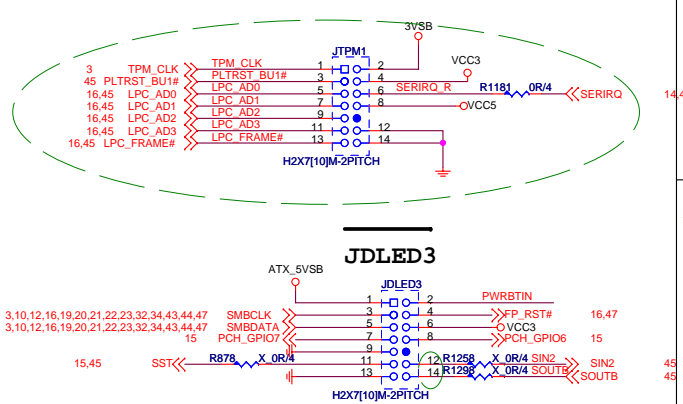
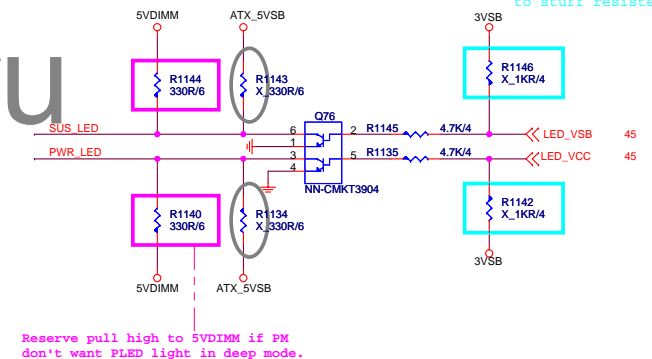
Turbo Button

TURBO_MODE#
Default: HIGH,disable OC
Push Bottom: LOW,Enable OC / Turn on LED

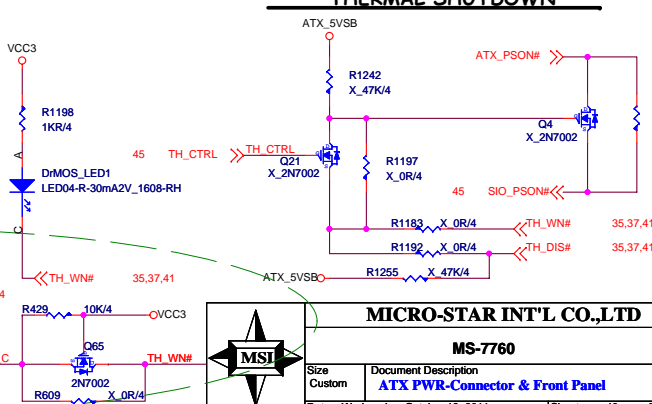
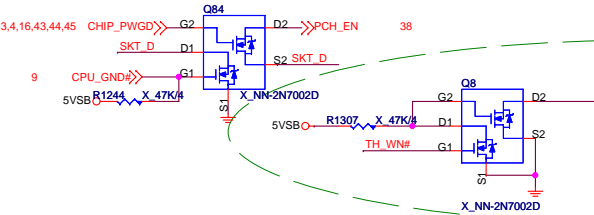
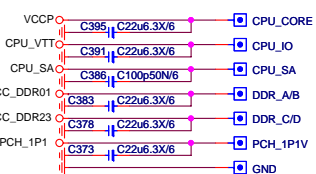


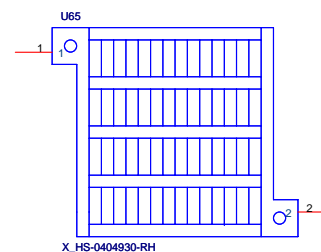
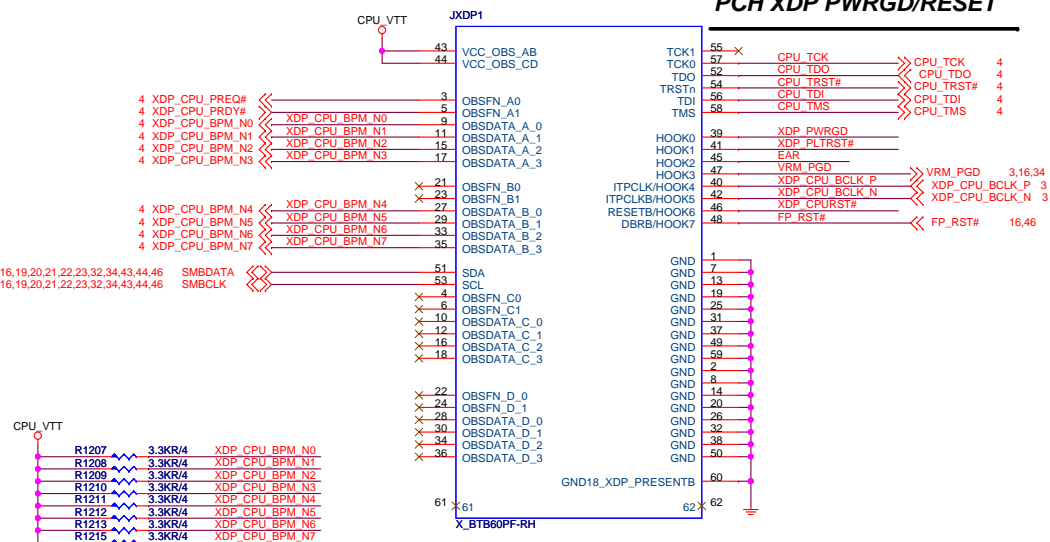
LED (for Fintek 71889)

SIO ver. LAA
Push pull pin, no need
to stuff resistors.

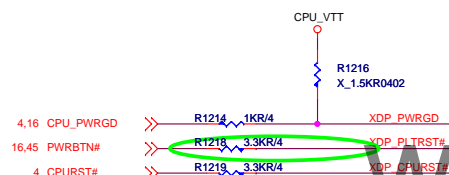
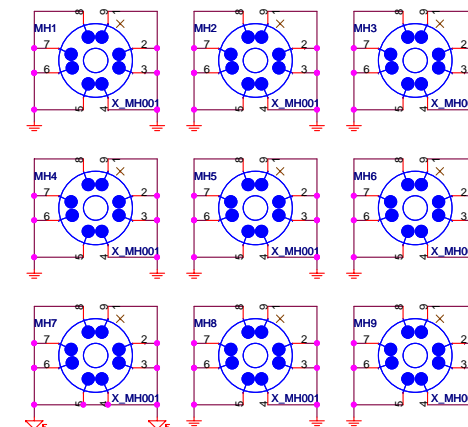


V-Check Points

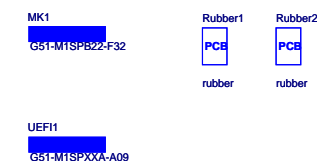
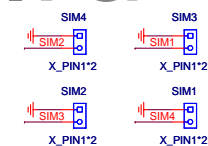




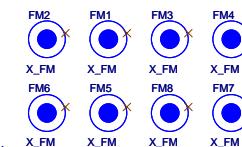
Mounting Holes



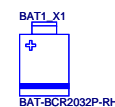
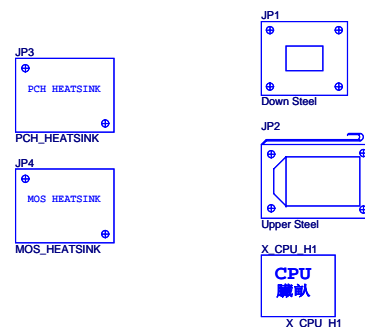
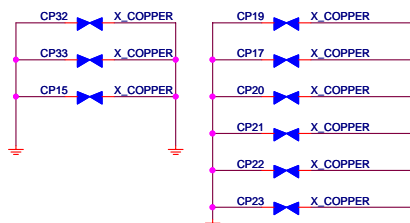
Simulation



Optical Fiducial Marks-120



Optical Fiducial Marks-100



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